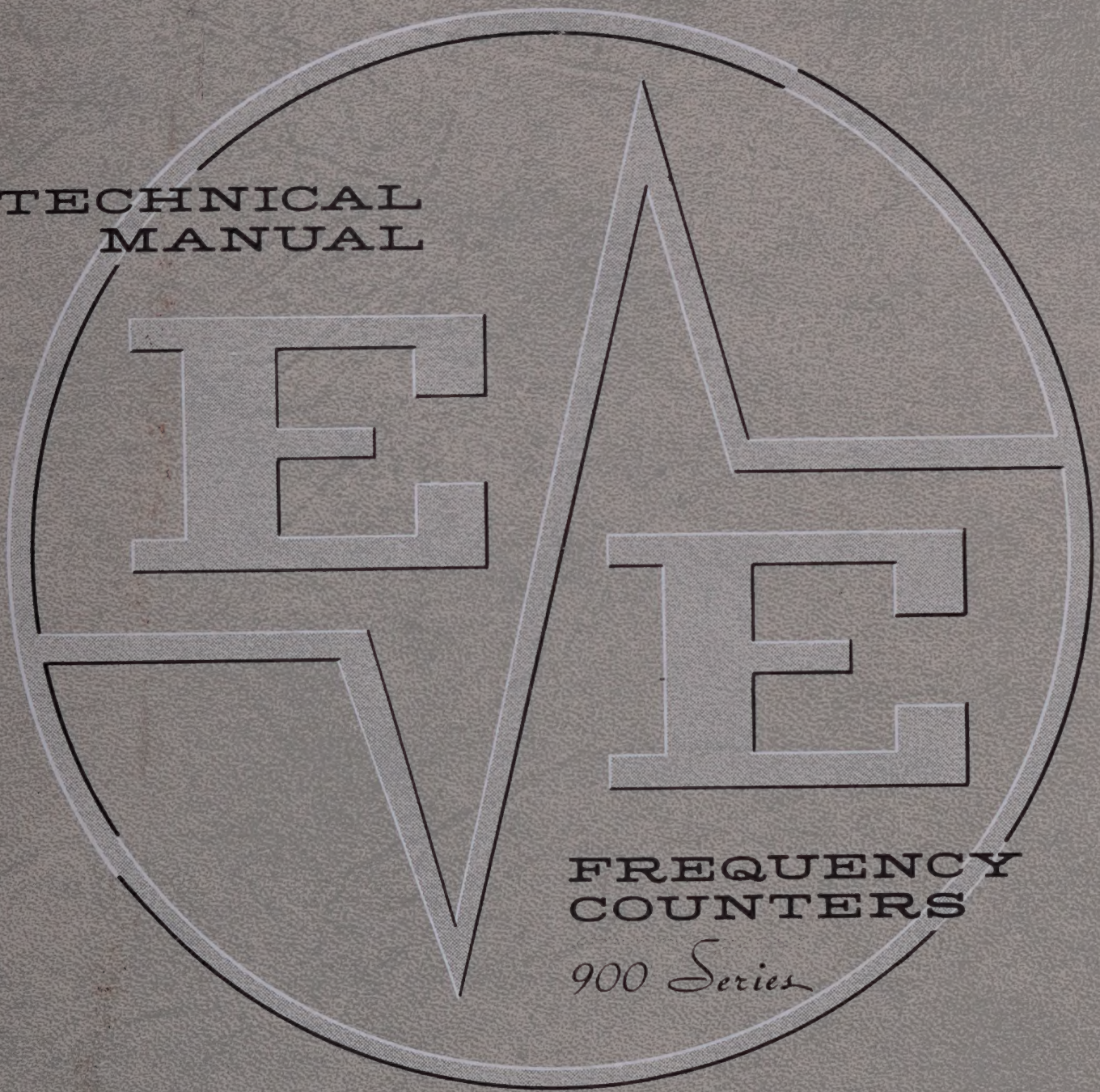
MESA ANTENNA
BLDG 42 OFFICE

TECHNICAL MANUAL



FREQUENCY COUNTERS

900 Series

ELDORADO ELECTRONICS
601 Chalomar Road, Concord, CALIFORNIA 94520
Telephone: 415-686-4200; Twx 415-687-3230

945

951

Technical Manual
900 Series Frequency Counters

Model 945: 4 GHz, 7 DIGIT Readout
Model 946: 4 GHz, 9 DIGIT Readout
Model 950: 6 GHz, 7 DIGIT Readout
Model 951: 6 GHz, 9 DIGIT Readout

ELDORADO ELECTRONICS
601 Chalomar Road, Concord, CALIFORNIA 94520
Telephone: 415-686-4200; Twx 415-687-3230

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ELDORADO ELECTRONICS
601 Chalomar Road, Concord, CALIFORNIA 94520

This Manual is packaged with instrument Serial Number 231

This Instrument is a

- MODEL 945 ☐
- MODEL 946 ☐
- MODEL 950 ☐
- MODEL 951 ☐

It contains options

- OPTION A ☑
- OPTION B ☐
- OPTION D ☐
- OPTION F ☑
- OPTION I ☐
- OPTION N ☐
- OPTION P ☑
- OPTION S ☐
- OPTION T ☐

Special Modification Number _____

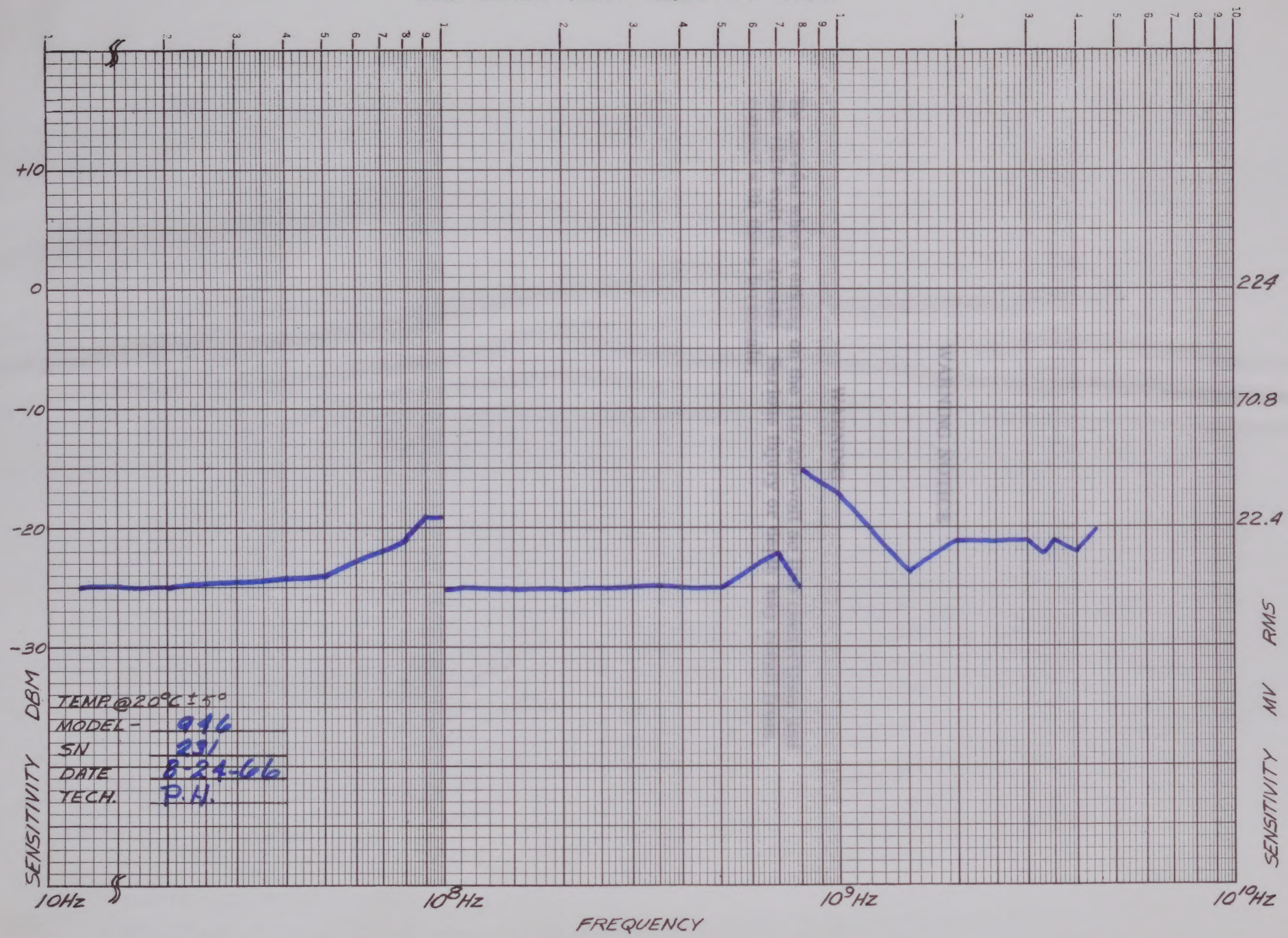
See Specification sheet and option description page for details.

This manual contains a

- MIL Standard Parts List ☐
- Commercial Parts List ☑

ORIGINAL

900 SERIES INPUT SENSITIVITY GRAPH



200 SERIES INPUT SENSITIVITY GRAPH

FREQUENCY

10 KHz 100 KHz 1 MHz 10 MHz

SENSITIVITY DBM

+10 0 -10 -20 -30

MODEL - 211 SERIAL# 1120

TECH. DATE

SENSITIVITY VS BAND

A.S.S. B.O.T. A.S.S.

WARNING NOTICE

WARNING

Be careful when working on the 115/220-volt ac line connections and the +330-volt dc circuits. Serious injury or death may result from contact with these terminals.

TABLE OF CONTENTS

CHAPTER 1.		INTRODUCTION	PAGE
Section	I.	General	
	1.	Scope	1
Section	II.	Description and Specifications	
	2.	Purpose and Use	3
	3.	Technical Specifications 945/946	3
	4.	Technical Specifications 950/951	8
	5.	Components of Frequency Counter	12
	6.	Description of Frequency Counter	13
	7.	Description of Option Codes	14
CHAPTER 2.		INSTALLATION	
Section	I.	Service Upon Receipt of Equipment	
	8.	Unpacking	15
	9.	Checking Unpacked Equipment	15
	10.	Tools and Test Equipment Required for Installation	15
	11.	Installation of Equipment	15
	12.	Equipment Cabling	16
Section	II.	Initial Adjustments of Equipment	
	13.	Extent of Initial Adjustments	22
CHAPTER 3.		OPERATING INSTRUCTIONS	
Section	I.	Operator's Controls and Indicators	
	14.	General	23
	15.	Operating Controls and Indicators	24
	16.	Measurement Error Indication	24

TABLE OF CONTENTS (Cont.)

			PAGE
CHAPTER 4.		THEORY OF OPERATION	
Section I.		General	
	17.	Scope	33
	18.	Terminology and Pulse Identification	33
	19.	Typical Basic Circuits	36
Section II.		Principals of Operation	
	20.	General	53
	21.	Frequency Measurement Technique	53
	22.	Simplified Block Diagram	65
	23.	Detailed Block Diagram	71
	24.	Operating Modes	71
	25.	Direct Mode Frequency Measurement Cycle	71
	26.	Mid-High Mode Frequency Measurement Cycle	75
Section III.		Unit Theory of Operation	
	27.	General	87
	28.	Circuit Description	87
CHAPTER 5.		MAINTENANCE	
Section I.		Preventive Maintenance	
	29.	General	133
	30.	Preventive Maintenance	133
	31.	Preventive Maintenance Checks	133
	32.	Cleaning of the Frequency Counter	133
Section II.		Performance Checks	
	33.	General	137
	34.	Test Equipment Required	137
	35.	Test Equipment, Tools, and Material	137
	36.	Performance Checkout Procedure	138
Section III.		Troubleshooting	
	37.	General	143
	38.	Troubleshooting	143
	39.	Troubleshooting Procedures	143

ORIGINAL

TABLE OF CONTENTS (Cont.)

			PAGE
	40.	Localizing Troubles	145
	41.	Test Setup	145
CHAPTER 6.		REPAIRS AND CALIBRATION	
Section I.		Repairs	
	42.	General	165
	43.	Parts Replacement Techniques	165
	44.	Parts Removal and Replacement Procedures	165
Section II.		Calibration	
	45.	General	169
	46.	Calibration Procedures	169
CHAPTER 7.		IDENTIFICATION TABLE OF PARTS	
Section I.		General	
	47.	General	179
	48.	Ordering Information	179
	49.	Code List of Manufacturers	179
	50.	Unit Numbering Method	181
Section II.		Schematic Drawing and Component Location	219

LIST OF ILLUSTRATIONS

FIGURE		PAGE
1.	Frequency Counter Packaging	17
2.	Frequency Counter, Controls and Indicators 945/950	27
3.	Frequency Counter, Controls and Indicators 946/951	31
4.	Frequency Counter Timing Functions	37
5.	Typical Diode Gate Circuit Functions	39
6.	Transistor Operation	43
7.	Basic Transistor Circuits	45
8.	Basic Four Binary Counter and Timing Functions	51
9.	Sampler Counter, Block Diagram	55
A.	Conventional Frequency Counter, Simplified Block Diagram	54
B.	Input Sampling Circuit, Simplified Block Diagram	57
C.	Astable MVB Output Adjusted for Stable Operation	58
D.	Simplified Input Sampler Circuit	58
E.	Sampler Output Without Slewing	59
F.	Sampler Output With Slewing	60
G.	f/N + 1.5 KHz Output, Simplified Logic Diagram	60
H.	Vector Addition of f/N and Δf	61
I.	Addition of f/N and Δf	63
J.	N Gating Simplified Block Logic	64
10.	Frequency Counter, Simplified Block Diagram	69
11.	Frequency Counter, Low Band of Operation Block Diagram	73
12.	Time Base Generator Timing Functions	83
13.	Frequency Counter 900 Series, Detailed Block Diagram	85
14.	25 MHz Decade Counting Unit, Block Diagram & Timing Functions	89
15.	2.5 MHz Decade Counting Unit, Block Diagram & Timing Functions	91
16.	250 KHz Decade Counting Unit, Block Diagram & Timing Functions	93
17.	Matrix Circuit, Block Diagram and Timing Functions	97
18.	Memory Readout, Block Diagram	101
19.	A.D. Circuit, $\div$ 16, $\div$ 8, and Ramp Generator, Block Diagram	103
20.	A Logic, Block Diagram and Timing Functions	107
21.	B Logic, Block Diagram and Timing Functions	109

LIST OF ILLUSTRATIONS (Cont.)

FIGURE		PAGE
22.	Parity Logic, Block Diagram	111
23.	Ratio and Control Circuit, Block Diagram	115
24.	Reset Circuit, Block Diagram and Timing Functions	119
25.	Time Base Delay Circuit, Block Diagram	121
26.	Overflow Circuit, Block Diagram	125
27.	Power Supply Assembly, Block Diagram	131
28.	25 MHz Decade Counting Unit, Schematic Diagram and Component Location	219
29.	2.5 MHz Decade Counting Unit, Schematic Diagram and Component Location	221
30.	250 KHz Decade Counting Unit, Schematic Diagram and Component Location	223
31.	Matrix Circuit, Schematic Diagram and Component Location	225
32.	Memory Readout, Schematic Diagram and Component Location	227
33.	A.D. Circuit and Divide-by-eight, Schematic Diagram and Component Location	229
34.	Divide-by-16, Schematic Diagram and Component Location	231
35.	Ramp Generator, Schematic Diagram and Component Location	233
36.	A Logic, Schematic Diagram and Component Location	235
37.	B Logic, Schematic Diagram and Component Location	237
38.	Parity Logic, Schematic Diagram and Component Location	239
39.	Ratio and Control Circuit, Schematic Diagram and Component Location	241
40.	Reset Circuit, Schematic Diagram and Component Location	243
41.	Time Base Delay Circuit, Schematic Diagram and Component Location	245
42.	Overflow Circuit, Schematic and Component Location	247
43.	Power Supply, Schematic Diagram	249
44.	Power Supply Regulator, Schematic Diagram & Component Location	251
45.	Decimal Point Readout Switch Connections	253
46.	Top Assembly and Component Location 945/950	255
47.	Top Assembly and Component Location 946/951	257
48.	Logic Chassis, Bottom View Component Location	259
	Eldorado Electronics Representatives	261

Chapter 1

INTRODUCTION

Section I GENERAL

1. SCOPE

This manual describes the Model 900 Series Frequency Counters. Instructions are given for installation, operation, theory, and maintenance. The manual also includes operation under unusual conditions, cleaning and inspection, replacement of parts, troubleshooting, calibration, and repair.

2. PURPOSE AND USE

a. The frequency counter is a bench or rack mountable instrument designed to automatically measure and display a broad frequency range in three overlapping bands. Eldorado's 900 series Frequency Counters* make precision frequency operations and calculations. The instruments use a completely new concept in high frequency counting that eliminates the need for heterodyning, transfer oscillator, or prescaling techniques.

b. Connecting the unknown frequency source to the counter, adjusting the trigger level and setting a three position range switch is all that is required for taking measurements. Correct readings appear within milliseconds instead of the minutes that are usually required to find the proper harmonic on other frequency measuring counters. Model 900 series provides true digital readout accuracy with no measurement ambiguity. The visual display indicates either zeros or the absolute reading, ±1 count.

c. The counter eliminate operator error by reading out only when the range switch is on the correct frequency band. Even the trigger level is automatically adjusted when equipped with Option A. A unique digital parity check feature monitors and rejects those readings that are inconsistent due to noise, or low input signal level.

d. The counter is a completely solid-state instrument with typical input signal sensitivity of 10 to 225 millivolts rms, into 50 ohms. Visual readout is by inline NIXIE (R) tube with display storage. Digital recorder signals for all digits plus a decimal point are simultaneously available in binary coded decimal format at a rear panel connector. Basic accuracy of the 900 series is ±1 count, ± oscillator stability.

e. Applications for the 900 series Frequency Counters include direct readings from high frequency transmitters, receivers, and oscillators; calibration of laboratory instruments; and high frequency stability measurements.

3. TECHNICAL SPECIFICATIONS MODELS 945/946

Input Frequency Range:

Low Band	20 Hz to 100 MHz
Mid Band	100 MHz to 800 MHz
High Band	800 MHz to 4 GHz
	10% Overlap between bands

Resolution 945:

Low Band	10 Hz
Mid and High Band	1 KHz

* Patents Pending

(R) Burroughs Corporation

Resolution 946 (Switch Selectable):	
Low Band	0.1, 1, 10, and 100 Hz
Mid and High Band	10 and 100 Hz, 1 and 10 KHz
Accuracy:	±1 count ± oscillator stability
Oscillator Stability 945 (Option B):	
Short Term	$5x10^{-8}$ per day (average)
Long Term (aging rate)	$3x10^{-7}$ per week after 24 hours
Temperature	$\pm5x10^{-9}$ per °C (0° to 52°C).
Oscillator Stability 946 (Option D):	
Short Term	$\pm5x10^{-10}$ per ten second interval and $5x10^{-9}$ per day.
Long Term (aging rate)	$2x10^{-8}$ per week after 24 hours
Temperature	$\pm2x10^{-10}$ per °C (0°C to 52°C)
Input Channel:	
Sensitivity:	
20 Hz to approximately 3.5 GHz	50mV rms into 50 ohms (-13 dBm, 0.05 mW) nominal
3.5 to 4 GHz	decrease to 224 mV rms (0 dBm, 1 mW) maximum
Dynamic Range:	Typically greater than 20 dB
Nondamaging overload:	2.2V rms into 50 ohms (+20 dBm, 100mW) maximum
Impedance:	50 ohms, VSWR typically less than 1.5:1
Connector:	Precision stainless steel type N female, front panel
External Standard Input:	1 MHz, 1 to 5V rms into 1000 ohms; Ac coupled; type BNC female rear panel (common with INTERNAL MONITOR connector)
Display Period:	0.3 to 10 seconds variable plus infinite
Reset:	
Manual	Pushbutton, front panel
Automatic	Reset occurs automatically at end of display period.

Remote	4 to 10V positive pulse into 1000 ohms; 1 usec maximum rise time; 5 usec minimum duration. Type BNC female, rear panel.
Internal Monitor	1 MHz; 0.75V rms nominal from 1000 ohms source impedance; AC coupled; Type BNC female, rear panel (common with EXTernal standard input connector).
Printer Output 945:	
Code	1-2-4-8 positive true negative level BCD ("0" = -9 volts nominal. "1" = -0.3 volts nominal) for seven digits of measurement information and the decimal point. 6, 800 ohm source impedance. (If option F installed, eight digits.)
Print Command	Automatic negative going step at end of count cycle; 0 volts to -12 volts nominal with fall time of one microsecond; 10, 000 ohms source impedance referred to -12 volts.
Connector	Amphenol No. 57-40500 rear panel.
Compatibility 945:	
Digital Printers	Beckman Model 1453-53; CMC Model 410A with Option 4aEE. HP Model 562A with eight option 22 column boards (nine with Option F) and Option 30 BCD Input connector assembly; Monroe Models 10-40-M1-0 and 13-80-M1-0, eight columns, (twelve with Option F); Clary Models 7000 per SCD 7500-27 and 7500 per SCD 7500-30; Franklin Model 1200-8 (1200-9 with Option F) with reverse logic and connector adapter options.
Remote Indicator	Eldorado Model 411.

Printer Output 946:

Code	1-2-4-8 positive true negative level BCD ("0" = -9V nominal, "1" = -0.3V nominal) for nine digits of measurement information and the decimal point; 6800 ohm source impedance.
Print Command	Automatic negative going step at end of count cycle; 0v to -12v nominal; 10,000 ohm source impedance referred to -12v.
Connector	Amphenol No. 57-40500, rear panel.

Compatibility 946:

Digital Printers	Beckman Model 1453-53; CMC Model 410A with Option 4aEE; HP Model 562A with ten Option 32 column boards and Option 30 BCD Input Connector Assembly; Monroe Models 10-40-M1-0 and 13-80-M1-0, twelve columns; Clary Model 7000 per SCD 7500-27 and 7500 per SCD 7500-30; Franklin Model 1200-10 with reverse logic and connector adapter options.
Remote Indicator	Eldorado Model 411.
Visual Readout 945:	Seven-digit in-line, long-life digital display tubes; automatic decimal point positioning reading in MHz; amber circularly-polarized window filter; direct or stored presentation. On the Model 945 with Remote Preset Reset Option F overflow and/or preset-reset indication is supplemented by numeral 1 or 2 indicator lamps located to the left of the most significant display tube.
Visual Readout 946:	Nine-digit in-line long-life digital display tubes; automatic decimal point positioning reading in MHz; amber circularly-polarized window filter; direct or stored presentation. Also, count indicator lamp (C) is illuminated for duration of count cycle.

ORIGINAL

Environment:

Temperature	Operating (per MIL-E-4158C), 0°C to 52°C; Storage, -35°C to +71°C, (limited by presently available tunnel diodes).
Altitude	Per MIL-E-4158C; Operating, sea level to 10, 000'; Storage, sea level to 40, 000'.
Vibration	Designed to meet MIL-T-4807A, Method 1A.
Shock	Designed to meet MIL-T-4807A, Method 3A.
Bench Handling	Designed to meet MIL-T-4807A, Method 4A.

Mechanical:

Size	5 1/4" x 16 3/4" x 20 5/8" (HxWxD)
Weight	Net, 38 lbs; Shipping, 50 lbs.
Rack Mounting	Conforms to RETMA Standard SE-102 (5 7/32" x 19") with mounting ears attached.
Colors	Panel - light grey, Color No. 26492 per FED STD 595. Bezel - Blue-Grey, Color No. 35164 per FED STD 595. Lettering - Blue-Black, Color No. 25042 per FED STD 595.
Accessories Supplied	One 3-to-2 wire AC line adapter, two rack mounting ears, two extender boards.
Power Input	115 vac ±10%, 50-60 Hz, 100 watts (plus 15 watts crystal oven power).

Options 945/946

Remote Reset Preset:	Option F
Model 945	Permits presetting to any number from all zeros to 29999.900 MHz in increments of 0.1 MHz. The preset number is determined by BCD coded wiring of up to 22 lines to a common (set) line on a mating connector (Amphenol No. 57-30360) for the rear panel mounted Amphenol No. 57-40360 connector.

Model 946	Permits presetting to any number from all zeros to 999999.900 MHz in increments of 0.1 MHz. The preset number is determined by BCD coded wiring of up to 28 lines to a common (set) line on a mating connector (Amphenol No. 57-30360) for a rear panel mounted Amphenol No. 57-40360 connector
Probe Power	Option P. Front panel connector provides power for Tektronix P6032 Cathode-follower probe.

All 900 Series Options are listed in Table 2.

4. TECHNICAL SPECIFICATIONS MODELS 950/951

Input Frequency Range:

Low Band	20 Hz to 100 MHz
Mid Band	100 MHz to 800 MHz
High Band	800 MHz to 6 GHz 10% overlap between bands.

Resolution 950:

Low Band	10 Hz
Mid and High Band	1 KHz

Resolution 951 (Switch Selectable):

Low Band	0.1, 1, 10, and 100 Hz
Mid and High Band	10 and 100 Hz, 1 and 10 KHz

Accuracy ..... ±1 count ± oscillator stability

Oscillator Stability 950: (Option B)

Short Term	5×10^{-8} per day (average)
Long Term (aging rate)	3×10^{-7} per week after 24 hours
Temperature	$\pm 5 \times 10^{-9}$ per °C (0°C to 52°C)

Oscillator Stability 951: (Option D)

Short Term	$\pm 5 \times 10^{-10}$ per ten second interval and 5×10^{-9} per day
Long Term (aging rate)	2×10^{-8} per week after 24 hours
Temperature	$\pm 2 \times 10^{-10}$ per °C (0°C to 52°C)

Input Channel:	
Sensitivity:	
20 Hz to approximately 4.5 GHz	50 mV rms into 50 ohms (-13 dBm, 0.05 mW) nominal
4.5 to 6 GHz.....	decrease to 224 mV rms (0 dBm, 1 mW) maximum
Dynamic Range:	Typically greater than 20 dB
Nondamaging Ove rload:.....	2.2V rms into 50 ohms (+20 dBm, 100 mW) maximum
Impedance:	50 ohms, VSWR typically less than 1.5:1
Connector:	Precision stainless steel type N female, front panel
External Standard Input:	1 MHz, 1 to 5V rms into 1000 ohms; AC coupled; type BNC female rear panel (Common with INTERNAL MONITOR connector)
Display Period:	0.3 to 10 seconds variable plus infinite
Reset:	
Manual:	Pushbutton, front panel
Automatic:	Reset occurs automatically at end of display period
Remote:	4 to 10V positive pulse into 1000 ohms; 1 usec maximum rise time; 5 usec minimum duration. Type BNC female, rear panel
Remote Preset Reset:	Option F (included standard)
Model 950.....	Permits presetting to any number from all zeros to 29999.900 MHz in increments of 0.1 MHz. The preset number is determined by BCD coded wiring of up to 22 lines to a common (set line on a mating connector (Amphenol No. 57-30360) for the rear panel mounted Amphenol No. 57-40360 connector.
Model 951.....	Permits presetting to any number from all zeros to 999999.900 MHz in increments of 0.1 MHz.

	The preset number is determined by BCD coded wiring of up to 28 lines to a common (set) line on a mating connector (Amphenol No. 57-30360) for a rear panel mounted Amphenol No. 57-40360 connector.
Internal Monitor:	1 MHz; 0.75V rms nominal from 1000 ohms source impedance; AC coupled; type BNC female, rear panel (common with EXTernal standard input connector)
Probe Power:	Option P. (Included Standard.) Front panel connector provides power for Tektronix P6032 Cathode-follower probe.
Printer Output 950:	
Code	1-2-4-8 positive true negative level BCD ("0" = -9 volts nominal, "1" = -0.3 volts nominal) for eight digits of measurement information and the decimal point. 6,800 ohm source impedance.
Print Command	Automatic negative going step at end of count cycle one microsecond fall time; 0 volts to -12 volts nominal; 10,000 ohms source impedance referred to -12 volts.
Connector	Amphenol No. 57-40500 rear panel
Compatibility 950:	
Digital Printers	Beckman Model 1453-53; CMC Model 410A with Option 4aEE; HP Model 562A with nine Option 22 column Boards and Option 30 BCD Input Connector Assembly; Monroe Models 10-40-M1-0, and twelve columns; Clary Models 7000 per SCD 7500-27 and 7500 per SCD 7500-30; Franklin Model 1200-9 with reverse logic and connector adapter options.
Remote Indicator	Eldorado Model 411.

Printer Output 951:

Code	1-2-4-8 positive true negative level BCD ("0" = -9v nominal, "1" = -0.3v nominal) for nine digits of measurement information and the decimal point; 6800 ohm source impedance.
Print Command	Automatic negative going step at end of count cycle one microsecond fall time; 0v to -12v nominal; 10,000 ohm source impedance referred to -12v.
Connector	Amphenol No. 57-40500, rear panel

Compatibility 951:

Digital Printers	Beckman Model 1453-53; CMC Model 410A with Option 4aEE; HP Model 562A with ten Option 22 column Boards and Option 30 BCD Input Connector Assembly; Monroe Models 10-40-M1-0 and 13-80-M1-0, twelve columns; Clary Models 7000 per SCD 7500-27 and 7500 per SCD 7500-30; Franklin Model 1200-10 with reverse logic and connector adapter options.
Remote Indicator	Eldorado Model 411.
Visual Readout 950	Seven-digit, in-line, long-life digital display tubes; automatic decimal point positioning reading in MHz; amber circularly-polarized window filter; direct or stored presentation. Overflow and/or preset-reset indication is supplemented by numeral 1 or 2 indicator lamps located to the left of the most significant display tube.
Visual Readout 951	Nine-digit in-line, long-life, digital display tubes; automatic decimal point positioning reading in MHz, amber circularly-polarized window filter direct or stored presentation. Also, count indicator lamp (C) is illuminated for duration of count cycle.

Environment:

Temperature	Operating (per MIL-E-4158C), 0°C to 52°C; Storage, -35°C to +71°C (limited by presently available tunnel diodes.
Altitude	Per MIL-E-4158C; Operating, sea level to 10, 000'; Storage, sea level to 40, 000'.
Vibration	Designed to meet MIL-T-4807A, Method 1A.
Shock	Designed to Meet MIL-T-4807A, Method 3A.
Bench Handling	Designed to meet MIL-T-4807A, Method 4A.

Mechanical:

Size	5 1/4" x 15 3/4" x 20 5/8" (H x W x D)
Weight	Net, 38 lbs; Shipping, 50 lbs.
Rack Mounting	Conforms to RETMA Standard SE-102 (5 7/32" x 19") with mounting ears attached.
Colors	Panel - Light Grey, Color No. 26492 per FED STD 595. Bezel - Blue-Grey, Color No. 35164 per FED STD 595. Lettering-Blue-Black, Color No. 25042 per FED STD 595.
Accessories Supplied	One 3-to-2 wire AC line adapter, two rack mounting ears, two extender boards (one Type N, female to GR874 adapter and one Amphenol No. 57-30360 connector).
Power Input:	115 vac ±10%, 50-60 Hz, 100 watts (plus 15 watts crystal oven power.)

All 900 Series Options are listed in Table 2.

5. COMPONENTS OF FREQUENCY COUNTER

The components shipped with the equipment are listed in Table 1.

Table 1. Frequency Counter and Accessories

Qty.	Item	Dimensions (in) Height	Depth	Width	Unit Weight (lb.)	Figure No.
1	Frequency Counter	5 1/4	17 1/4	16 3/8	38	1
2	Mounting Ears	-	-	19	1	1
2	PC Board Extenders	-	-	-	1/4	1
1	AC Line Ground Adapter Models 950/951	-	-	-	1/4	1
1	Cable Connector	-	-	-	1/4	1
1	Adapter Type N, female to GR 874	-	-	-	1/4	1

6. DESCRIPTION OF FREQUENCY COUNTER

a. The series 900 Frequency Counters are of all solid state construction designed to automatically measure and display input signals over a wide frequency range. Direct readout of the input frequency is accomplished by a unique measuring technique perfected by Eldorado. All necessary operating controls are located on the front panel.

b. The frequency counter operates over three wide, switch-selected, frequency bands. Operation is such that the readout display will show the input frequency or all zeros. An all zero reading is caused by either, the range switch being in the wrong position for the input frequency or the parity circuit check is rejecting the signal.

c. The input frequency is displayed on in-line, long-life digital indicators with a decimal point automatically positioned to indicate the input frequency in MHz.

d. Display time duration is variable with either a Direct or Stored display mode. In the stored mode of operation only the input frequency changes are seen on the readout indicators. In the Direct mode the totalization of the input frequency during the count cycle is seen on the indicators. During the display period a print command signal reads out the BCD coded information.

e. Parity control allows the operator to select an optimum operating level for inconsistent signals due to noise, excessive modulation or low amplitude. In normal operation parity is set for maximum. The frequency to be read out is then monitored for consistency and if the consistency criteria is not met the signal is rejected. By means of the parity control the operator reduces the effectiveness of the parity circuits and allows the counter to read out a random group of frequencies. A pattern of these readings will be observed appearing around a center reading. Thus difficult to monitor signals may be used.

f. Input sensitivity is adjusted by a trigger Manual control. On instruments including Option A, a choice of Manual or Automatic trigger control is available. In the automatic mode the trigger level is set by the parity circuit automatically to the optimum operating level.

g. For frequency measurements requiring high isolation between source and instrument Option P (included standard on 950/951) provides a convenience jack supplying power to a Tektronix high impedance cathode follower probe. Typical characteristic of this probe are, DC input resistance 10 megohms, DC input capacitance 3.6 pf, frequency response 3 db to 850 Mc. See Tektronix instruction manual P6032 Probe for details.

h. The time base is referenced to a one-megahertz, temperature stabilized crystal oscillator. The one-megahertz crystal oscillator provides the master clock reference for all frequency measurements. The crystal oven heating element is connected to the power input cable (bypassing the power switch) to assure long-term stability of the crystal frequency in normal operation. (If the crystal is cooled the aging cycle is re-instated.)

7. DESCRIPTION OF OPTION CODES

a. The 900 Series Frequency Counters are designed for optimum versatility, simple operation and reliability. All instruments offer microwave frequency counting, high speed, error-free measurements, digital accuracy, high sensitivity, no calculations, and unequaled operating ease.

b. Option Table 2 shows the added features available for each instrument. An option listed as included indicates this is a standard feature of that instrument.

Table 2. Options Available Per Instrument

OPTION	DESCRIPTION	INSTRUMENTS			
		945	946	950	951
A	Automatic Trigger Level	x	x	included	included
B	Lower stability Crystal, same stability specified for Models 945 and 950.		x		x
D	High stability Crystal, same stability specified for Models 946 and 951.	x		x	
F	Remote Preset Reset	x	x	included	included
I	RFI (per MIL-I-6181D, -16910A -26600)	x	x	x	x
N*	Input Connector Rear Panel	x	x	x	x
P*	Probe Power for Tektronix P6032	x	x	included	included
S	230 vac ±10%, 50-60 Hz operation without cable plug	x	x	x	x
T	115 vac ±10%, 50 - 400 Hz operation	x	x	x	x

*Option N and Option P are not available in combination because the Tektronix Probe requires the input connector be located adjacent to the probe power connector. Therefore, if Option N is installed on Models 950/951, Option P is eliminated.

Chapter 2

INSTALLATION

Section I SERVICE UPON RECEIPT OF EQUIPMENT

8. UNPACKING

The frequency counter is shipped in a specially constructed container to provide maximum protection to the equipment during transit. Use care when unpacking to prevent damage to the equipment, such as the cabinet paint finish, controls, indicators, connectors, etc.

a. Packaging Data. When packed for shipment, the frequency counter is placed in a carton and packed in a corrugated shipping box. A typical shipping box and its contents is shown in figure 1. The dimensions, volume, and contents of the shipping boxes are listed in Table 3.

Table 3. Packaging Data

Box No.	Contents	Dimensions (in.)	Volume (cu, ft.)	Weight (lb.)
1	Frequency Counter, Manual & accessories	9 x 24-1/2 x 24-1/2	29	50

9. CHECKING UNPACKED EQUIPMENT

a. Inspect the equipment for damage incurred during shipment. If the equipment has been damaged, report damage immediately to the carrier, so that inspection may be made and a claim filed.

b. See that the equipment is complete as listed on the packing slip. If a packing slip is not available, check the equipment against Table 1 Frequency Counter and Accessories.

10. TOOLS AND TEST EQUIPMENT REQUIRED FOR INSTALLATION

No special tools or test equipment are required for installation.

11. INSTALLATION OF EQUIPMENT

a. Frequency Counter, Bench Mounting. The frequency counter is ready for bench mounting after unpacking is completed. No additional assembly is required.

b. Frequency Counter, Rack Mounting. The frequency counter is normal package for bench mounting. If the unit is to be installed in a rack proceed as follows:

(1) Remove rack ears from accessory package.

(2) Remove nylon screws from the side panels.

(3) Fasten rack ears in position with mounting screws supplied.

(4) Remove blank panel in rack where frequency counter is to be mounted. Retain hardware.

(5) Install frequency counter in rack using mounting screws previously removed.

(6) Install the cable connections as detailed in paragraph 12.

12. EQUIPMENT CABLING

The frequency counter is shipped ready for use except for signal input cabling.

CAUTION: If the Frequency Counter contains Option I, all external connections should be by RFI shielded cable including Printer output, and Preset cabling. The instrument cabinet design including power cord meets RFI specifications. Any customer furnished cable must be shielded.

a. Signal Input Cable. The input signal is supplied to the frequency counter through the Type N input connector.

b. Printer Output. The frequency counter may be used with a mechanical printer. The binary-coded-decimal output signals are available at the PRINTER OUTPUT connector A49J3. Cable for printers are normally supplied with the printer. If Option I is installed on the instrument, the printer and printer cable will not necessarily meet these specifications. Shielded cable should be used to conform to RFI specifications. Refer to Table 4 for connector pin wiring of printer output connector J3. The following printers are compatible with the Model 945:

(1) Beckman Model 1453-53

(2) CMC Model 410A with Option 4aEE

(3) HP Model 562A with eight option 22 column boards and option 30 BCD Input connector assembly. (Nine option 22 column boards if equipped with Option F.)

(4) Monroe Models 10-40-M1-0 and 13-80-M1-0 eight columns, twelve columns if equipped with Option F.

(5) Clary Models 7000 per SCD 7500-27 and 7500 per SCD 7500-30

(6) Franklin Model 1200-1 with reverse logic and connector adapter options. (1200-9 if equipped with Option F.)

The following printers are compatible with Models 946, 950, and 951:

(1) Beckman Model 1453-53

(2) CMC Model 410A with Option 4aEE

(3) HP Model 562A with ten Option 22 column boards and option 30 BCD input connector assembly. (Nine option 22 column boards for the Model 950.)

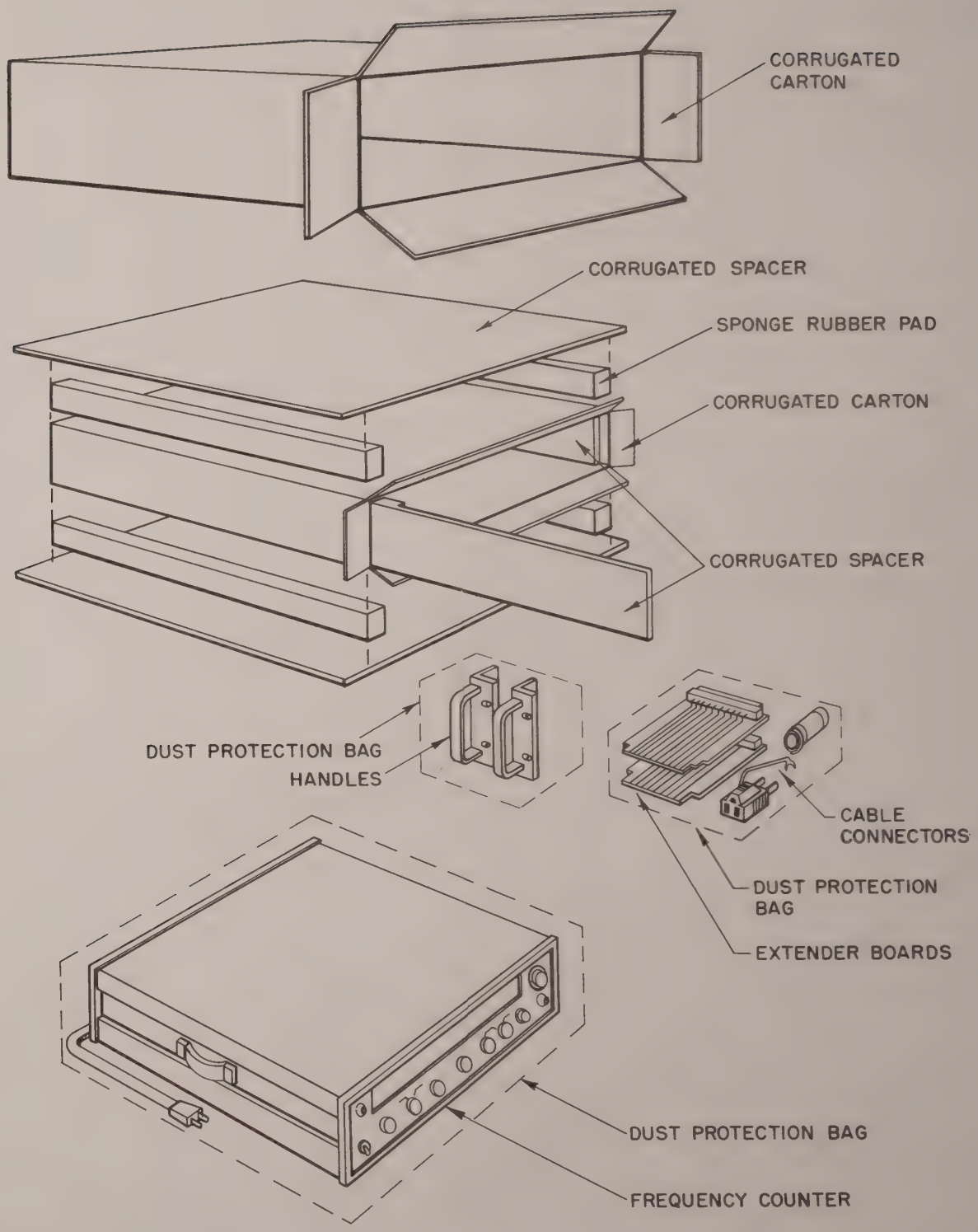


FIGURE 1. FREQUENCY COUNTER PACKAGING

(4) Monroe Models 10-40-M1-0 and 13-80-M1-0, twelve columns.

(5) Clary Models 7000 per SCD 7500-27 and 7500 per SCD 7500-30.

(6) Franklin Model 1200-10 with reverse logic and connector adapter options. (1200-9 with Model 950.)

The Eldorado Model 411 Remote Indicator is available and designed to repeat the visual presentation at a remote location.

c. Remote Preset Reset cable connections. Option F, which is included as standard on the Model 950 and 951 allows presetting to any desired number in increments of 0.1 MHz. The frequency counter is shipped without a remote preset reset cable but with a 36 conductor cable connector (57-30360) supplied with the counter. (If the instrument is supplied with Option I this cable should be shielded to meet the RFI specifications.) Refer to Table 5 for a wiring chart of the rear panel preset reset connector. Instructions for presetting to a desired number are found in Chapter 4, Section III, Theory of Operation, Remote Preset Reset Circuit.

d. Power Cable. The frequency counter is equipped with a three-wire power cable. After the instrument is installed and the signal input cables are connected, connect the power cable to any convenient 115 volt 60 cycle ac power outlet. The exposed portions of the instrument are grounded for safety. When only a two-blade outlet is available, use the power cable adapter supplied with the instrument. Connect the short wire from the side of the adapter to a convenient grounding point.

(1) When installed with Option T, 400 cycle operation is possible.

(2) When installed with Option S, 230V ac 50-60 Hz, the power cord is not equipt with a plug.

Table 4. Printer Output Wiring Table

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	10^{0} 1 bit	26	10^{0} 4 bit
2	10^{0} 2 bit	27	10^{0} 8 bit
3	10^{1} 1 bit	28	10^{1} 4 bit
4	10^{1} 2 bit	29	10^{1} 8 bit
5	10^{2} 1 bit	30	10^{2} 4 bit
6	10^{2} 2 bit	31	10^{2} 8 bit
7	10^{3} 1 bit	32	10^{3} 4 bit
8	10^{3} 2 bit	33	10^{3} 8 bit
9	10^{4} 1 bit	34	10^{4} 4 bit
10	10^{4} 2 bit	35	10^{4} 8 bit
11	10^{5} 1 bit	36	10^{5} 4 bit
12	10^{5} 2 bit	37	10^{5} 8 bit
13	10^{6} 1 bit	38	10^{6} 4 bit
14	10^{6} 2 bit	39	10^{6} 8 bit
15	10^{7} 1 bit	40	10^{7} 4 bit
16	10^{7} 2 bit	41	10^{7} 8 bit
17	10^{8} 1 bit	42	10^{8} 4 bit
18	10^{8} 2 bit	43	10^{8} 8 bit
19	Dec. Pt. 1 bit	44	Dec. Pt. 4 bit
20	Dec. Pt. 2 bit	45	Dec. Pt. 8 bit
21	Read	46	+300
22	+12	47	-12
23	+Print Command	48	- Print Command
24	-Ref. (-9v)	49	Inhibit (NoConnection)
25	Ground	50	Ground

NOTES:

1. 10^{0} is the least significant digit and appears as the digit farthest to the right.
2. Pin 24 (-9 volt reference) is from a resistor network consisting of 390 ohms in series with -12 volts with 1.8K ohms to ground.
3. Negative print command is a negative step from nominal 0 to -12 VDC at end of count cycle. Fall time is approximately 1 usec. The duration depends on display time and ranges from 100 millisec minimum to 10 seconds maximum. Source impedance is approximately 10 K ohms.
4. Positive print command is a positive step from nominal -3 VDC to +4 VDC at end of count cycle. Rise time is approximately 5 usec. The duration depends on display time and ranges from 100 millisec minimum to 10 seconds maximum. Source impedance is approximately 1 K ohms.
5. Read command is a positive pulse from a nominal -8 VDC to 0, 50 usec. in width. The leading edge of the pulse is coincident with the print command. Source impedance is approximately 600 ohms.
6. Output connector is Amphenol jack 57-40500. Mating connector is Amphenol plug 57-30500.
7. Unused digits are wired to print zero.

Table 5. Remote Preset Reset Wiring Table

PIN NO.	FUNCTION		PIN NO.	FUNCTION
1	10^2 1 bit		19	10^2 4 bit
2	10^2 2 bit		20	10^2 8 bit
3	10^3 1 bit		21	10^3 4 bit
4	10^3 2 bit		22	10^3 8 bit
5	10^4 1 bit		23	10^4 4 bit
6	10^4 2 bit		24	10^4 8 bit
7	10^5 1 bit		25	10^5 4 bit
8	10^5 2 bit		26	10^5 8 bit
9	10^6 1 bit		27	10^6 4 bit
10	10^6 2 bit		28	10^6 8 bit
11	10^7 1 bit	overflow lights	29	10^7 4 bit
12	10^7 2 bit		30	10^7 8 bit
13	10^8 1 bit		31	10^8 4 bit
14	10^8 2 bit		32	10^8 8 bit
15	A. Gen.		33	A. Gen.
16	Open		34	Gate
17	Ground		35	Ground
18	+12V		36	-12V

Notes:

As shown on the chart, the 10^0 and 10^1 functions are not preset. 10^0 is the least significant (most right-hand) digit. On the Models 945 and 950 the 10^7 function represents two overflow lights which can be preset to either "1" or "2". The wiring for any particular digit is performed in 1-2-4-8 code. For example, if reset to "1" in the 10^2 position is required, a connection is made between Pin 1 of the connector to either, or both, of the A generator pins 15 and/or 33. As an additional example, if it is desired to have the instrument reset to 7 in the 10^2 position, it would require wiring Pins 1, 2 and 19 to Pins 15 and/or 33 of the A generator.

In all cases, a wire should be made between Pins 18 and 34 which turns on an input gate in the A generator.

The 36 pin connector on the rear of the instrument is an Amphenol 5740360. The mating connector (supplied with the instrument) is an Amphenol 5730360.

13. EXTENT OF INITIAL ADJUSTMENTS

The frequency counter is fully automatic during operation. All controls required for operation are mounted on the front and rear panels. No additional adjustment of controls is required.

Chapter 3

OPERATING INSTRUCTIONS

Section I OPERATOR'S CONTROLS AND INDICATORS

14. GENERAL

a. This instrument makes precision microwave frequency measurements without complex, time-wasting operations and calculations. A new concept in high frequency measurement eliminates the need for heterodyne and transfer oscillators. Measurements are made in split seconds, and with none of the operator adjustments associated with conventional high frequency counters. By reading and printing out all digits and the decimal point, these counters eliminate any chance of immediate or future misinterpretation of measurement data.

b. These are the only direct counting GHz frequency counters offering high-speed, error-free measurements; digital accuracy; high sensitivity and unmatched operating ease. The only operations normally needed to make measurements with those models that include automatic trigger control are to connect the unknown frequency and set a three-position band switch. Operator fatigue is further reduced by display storage which permits the readout to change only when the input frequency varies. Also, the unique parity check circuit, which is designed to allow only correct readings to be displayed, virtually eliminates operator error.

c. The parity check circuit is adjustable and functions to monitor and compare successive measurements to determine the consistency of the input signal. In the minimum parity position, a no-consistency criterion is established; in the full parity position, maximum consistency is required. If the consistency criterion is not met, parity resets the counter and presents an all-zero reading. When operating in the auto-trigger mode, parity also controls the trigger level until a stable trigger point is obtained. Reduced parity allows the operator to manually evaluate input signal consistency.

d. Both the Model 950 and 951 incorporate preset reset circuitry to offset readings by a predetermined number. This feature permits direct readout of the input frequency to any heterodyne device providing the sum of the reference frequency and the difference frequency do not exceed the counter's capability. Preset reset is an optional item on the Models 945 and 946.

e. All four of the counters are reliable, rugged instruments that meet the military environmental specifications outlined elsewhere in this manual. Sound mechanical construction, solid-state components and glass epoxy PC boards all contribute to the design integrity of the 900 Series. Maintenance ease is built into the units by using conservative circuit designs, plug-in circuit boards and, where possible, off-the-shelf components. When equipped with Option I, these are the

only counters that meet the RFI requirements of MIL-I-6181D, MIL-I-16910A and MIL-I-266000.

f. The 900 Series Counters in effect offer automatic, foolproof microwave frequency measurements. Thus, they are ideally suited for applications in which rapid reading, unattended operation, or measurements by unskilled people are required. They are particularly adapted to systems use since, in any one band, all measurements can be made automatically with all digits and the decimal point being available in a parallel binary coded decimal format at a rear panel connector. For greater versatility, these counters are designed for compatibility with a wide variety of digital printers produced by numerous manufacturers (see "Specifications"). Also, the front-panel probe power jack provided on those Models with option P can be used in those applications that demand a high input impedance. Probe power is an optional item for the Models 945 and 946.

15. OPERATING CONTROLS AND INDICATORS

a. Front and rear panel controls and indicators for the Models 945/950 are shown in figure 2.

b. Front and rear panel controls and indicators for the Models 946/951 are shown in figure 3.

c. The controls name and function are listed in table 6 and table 7 for the 945/950 and 946/951 respectively.

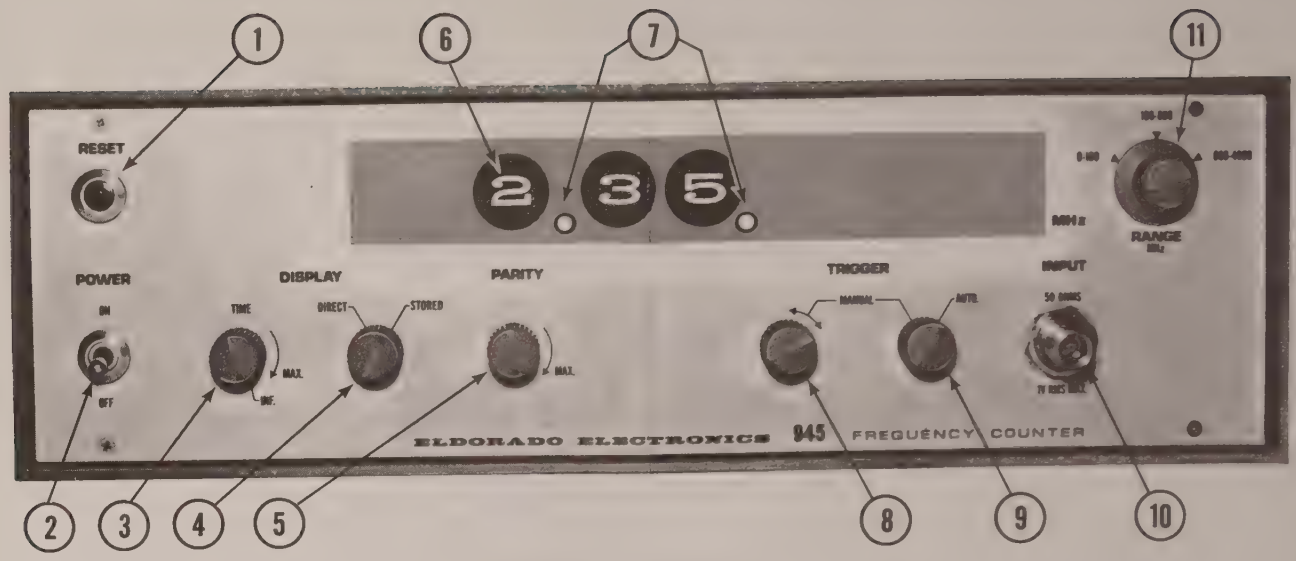
16. MEASUREMENT ERROR INDICATION

If a measurement error occurs (due to noise, low amplitude etc.) the parity consistency check will detect such errors and cause the frequency counter to display all zeros. If the instrument is programmed to a preset number (Option F), the preset number will appear rather than all zeros. Any continuous or erratic measurement error indications should be investigated. These may be due to a defective source or a malfunction within the instrument.

Table 6. Front and Rear Panel Operating Controls and Indicators 945/950

Control or Indicator	Function
POWER switch	In the ON position, turns on instrument.
TIME control	Sets display time period, continuously variable from 0.3 to 10 seconds. Maximum CW position activates a switch for infinite display time.
DIRECT-STORED switch	In the DIRECT position, indicators flash the count during sampling time. In the STORED position indicators remain fixed and change only with frequency variations.
PARITY control	Selects the number of input samples to be compared for consistency. Maximum parity (CW) is the normal setting.
MANUAL TRIGGER control	Sets input trigger level.
MANUAL AUTO TRIGGER switch	Option A. In MANUAL position trigger level is manually set. In AUTO position input trigger level is automatically adjusted to correct input level.
INPUT connector	Applies external frequency to be measured to instrument.
PROBE POWER connector	Option P. Supplies power for Tektronix P6032 high impedance cathode-follower probe.
RESET pushbutton	A manual method of resetting the instrument.
RANGE switch	A three-position switch to select input frequency range.
DIGITAL DISPLAY	Seven digit in-line digital frequency readout indicators.
DECIMAL POINT indicator	Automatically shifts, as range switch is varied to display the frequency measurement directly in MHz.
OVERFLOW INDICATORS	Indicate when the count capacity of the instrument has been exceeded. Can show up to three overflows by turning on indicator lamps. When option F is installed can be preset to extend counter readout to 8 digits (Models 945/950).
PRINTER OUTPUT connector	Provides 8-4-2-1 positive true negative level BCD ("0" = -9 volts nominal, "1" = 0.3 volts nominal) to digital recorders. Decimal point and eight digits of measurement information (seven digits Model 945 without Option F). See table 4.

INT/EXT MONITOR BNC connector.....	Provides a means to monitor the time base reference oscillator, or apply external 1MHz standard.
INT/EXT Time Base oscillator slide switch.....	In the INT position connects the internal reference crystal oscillator to time base circuitry and provides internal reference at rear BNC. In the EXT position removes internal oscillator and connects the rear BNC connector to the time base circuitry. Allows for external use of a 1MHz reference oscillator.
PRESET connector.....	Option F, allows presetting counter to any number from zero to 29999.900MHz. See table 5.
INPUT connector.....	Option N, connector is relocated to the rear panel. Probe Power connector is eliminated by this option.
REMOTE RESET connector.....	Provides for external reset control of the instrument.



MODEL 945/950

FRONT AND REAR PANEL CONTROLS

1. RESET BUTTON
2. POWER SWITCH
3. DISPLAY TIME CONTROL AND SWITCH
4. DISPLAY DIRECT OR STORED SWITCH
5. PARITY CONTROL
6. FREQUENCY DISPLAY INDICATORS
7. DECIMAL INDICATORS
8. MANUAL TRIGGER CONTROL
9. AUTO MANUAL TRIGGER SWITCH (OPTION A)
10. INPUT CONNECTOR
11. RANGE SWITCH
12. PRINTER OUTPUT CONNECTOR
13. INTERNAL OSCILLATOR MONITOR/EXTERNAL OSCILLATOR INPUT JACK
14. REMOTE RESET JACK
15. INTERNAL/EXTERNAL OSCILLATOR SWITCH
16. OPTION N
17. OPTION F

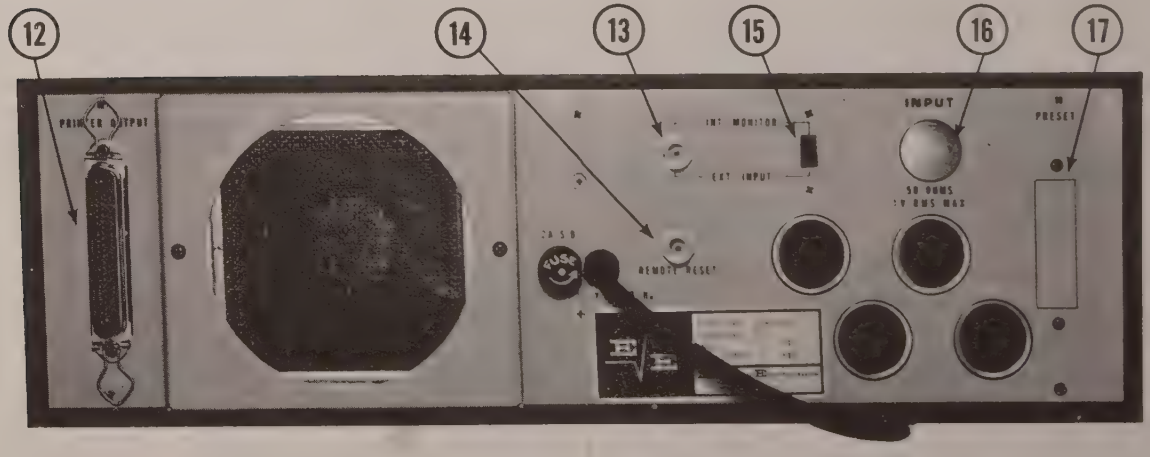
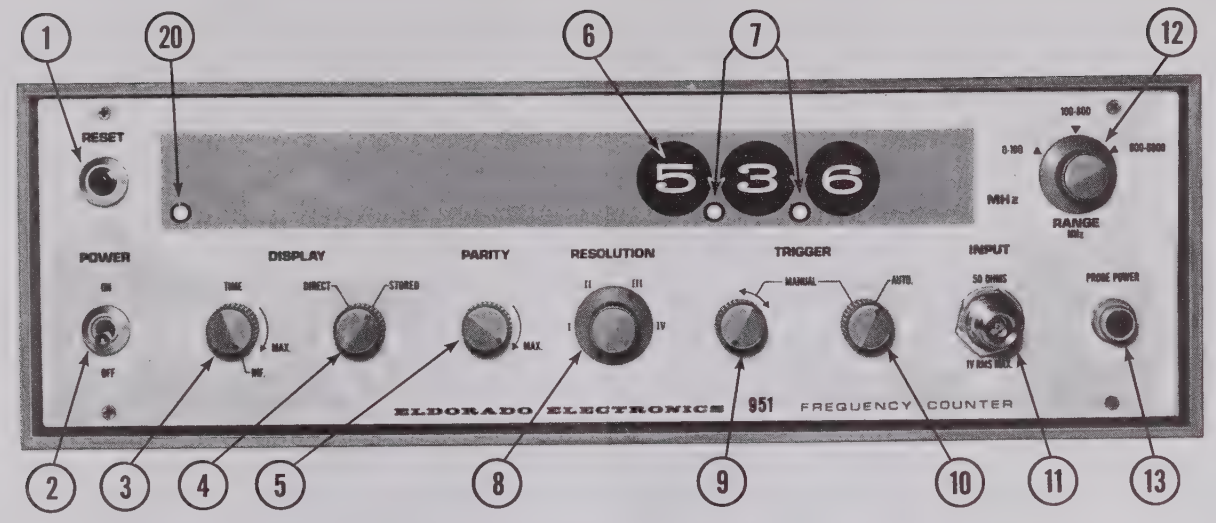


FIGURE 2 FRONT AND REAR PANEL CONTROLS

Table 7. Front and Rear Panel Operating Controls and Indicators 946/951

Control or Indicator	Function
POWER switch	In the ON position, turns on the instruments.
TIME control	Sets display time period, continuously variable from 0.3 to 10 seconds. Maximum CW position activates a switch for infinite display time.
DIRECT-STORED switch	In the DIRECT position, indicators flash the count during sampling time. In the STORED position indicators remain fixed and change only with frequency variations.
PARITY control	Selects the number of input samples to be compared for consistency. Maximum parity (CW) is the normal setting.
RESOLUTION	Four position switch to control the resolution of least significant digit. Resolution is .1, 1, 10, and 100 Hz on 0-100 MHz low band, for positions I, II, III and IV respectively. Display readout is 10Hz, 100Hz, 1KHz and 10KHz on midband and high band, for positions I, II, III and IV respectively.
MANUAL TRIGGER control	Sets input trigger level.
MANUAL AUTO TRIGGER switch	Option A, in MANUAL position trigger level manually set. In AUTO position input trigger level is automatically adjusted to correct input level.
INPUT connector	Applies external frequency to be measured to instrument.
PROBE POWER connector	Option P. Supplies power for Tektronix P6032 high impedance cathode-follower probe.
RESET pushbutton	A manual method of resetting the instrument.
RANGE switch	A three-position switch to select input frequency range.
DIGITAL DISPLAY	Nine-digit, in-line digital frequency readout indicators.
DECIMAL POINT indicator	Automatically shifts, as Range and/or Resolution switch is varied, to display the frequency measurement directly in MHz.
COUNT indicator	Time base count lamp indicates when counting chain is gated on and counting.

PRINTER OUTPUT connector.....	Provides 8-4-2-1 positive true negative level BCD ("0" = -9 volts nominal, "1" = -0.3 volts nominal) to digital recorders. Decimal point and nine digits of measurement information. (See table 4.)
INT/EXT MONITOR BNC connector.....	Provides a means to monitor the time base reference oscillator or apply external 1MHz standard.
INT/EXT Time Base oscillator slide switch.....	In the INT position connects the internal reference crystal oscillator to the time base circuitry and provide internal reference at rear BNC. In the EXT position removes internal oscillator and connects BNC connector to the time base circuitry. Allows for external use of a 1MHz reference oscillator.
PRESET connector.....	Option F, allows presetting counter to any number from zero to 999999.900 MHz. See table 5.
INPUT connector.....	Option N, Input connector is relocated on the rear panel. Probe power is eliminated by this option.
REMOTE RESET connector.....	Provides for external reset control of instrument.



MODEL 946/951

FRONT AND REAR PANEL CONTROLS

1. RESET BUTTON
2. POWER SWITCH
3. DISPLAY TIME CONTROL AND SWITCH
4. DISPLAY DIRECT OR STORED SWITCH
5. PARITY CONTROL
6. FREQUENCY DISPLAY INDICATORS
7. DECIMAL INDICATORS
8. RESOLUTION SWITCH
9. MANUAL TRIGGER CONTROL
10. AUTO MANUAL TRIGGER SWITCH (OPTION A)
11. INPUT CONNECTOR
12. RANGE SWITCH
13. PROBE POWER CONNECTOR
14. PRINTER OUTPUT CONNECTOR
15. INTERNAL OSCILLATOR MONITOR/EXTERNAL OSCILLATOR INPUT JACK
16. REMOTE RESET JACK
17. INTERNAL/EXTERNAL OSCILLATOR SWITCH
18. OPTION N
19. PRESET RESET CONNECTOR (OPTION F)
20. TIME BASE COUNT (C) LIGHT

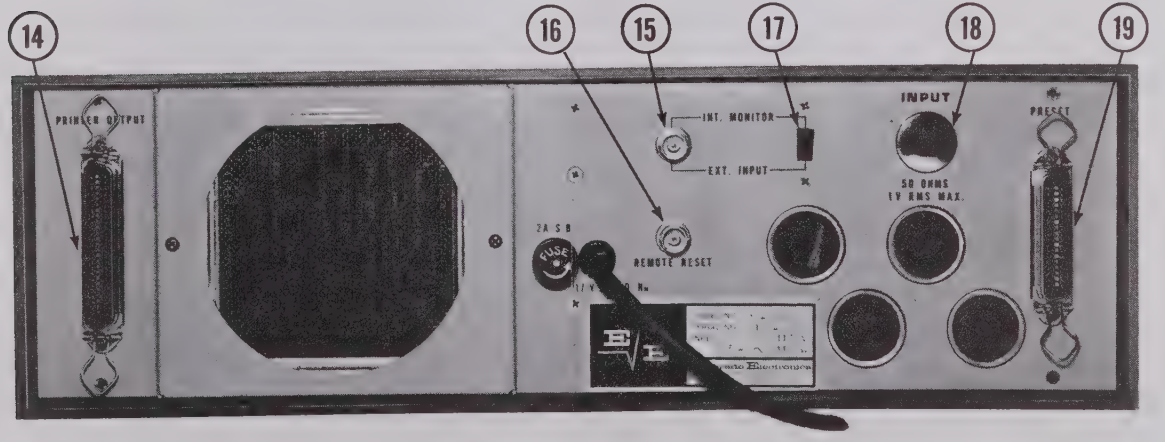


FIGURE 3 FRONT AND REAR PANEL CONTROLS

Chapter 4

THEORY OF OPERATION

Section I GENERAL

17. SCOPE

a. This chapter contains the theory of operation for the frequency counter circuits. Included are the simplified block diagram description, an overall block diagram description, and detailed block diagram level descriptions of the individual printed circuit boards.

b. Section I defines terminology used. Also contained in Section I are typical basic circuit descriptions and pulse function identifications used in the 900 Series frequency counter circuits.

18. TERMINOLOGY AND PULSE IDENTIFICATION

The following definitions of terms are used throughout the manual.

a. Counters

(1) Binary. A bistable multivibrator (flip-flop) used to divide an input frequency by two or to store binary information.

(2) Binary-Coded-Decimal. (BCD) decimal information is coded in such a way that each digit may be represented by a unique combination of the 1 and 0 states* of four binaries.

(3) Counting Unit. A series of binaries connected in cascade to provide for a frequency division of a predetermined amount.

(4) Decade Counting Unit. DCU or decimal counting unit, a series of binaries connected in cascade with gating to provide for a frequency division of ten.

(5) Decimal Weight. Numerical value assigned to the output of each binary. In a 1248 code, decimal weights are assigned as follows: A binary, 1; B binary, 2; C binary 4; D binary, 8.

(6) 1 State. One of a pair of transistor in a binary conducting and indicates decimal weight present.

*Note: The 1 state may be alternately described as the set state or the True condition. The 0 state may be alternately described as the Reset state or the False condition. These terms may be used interchangeably in this manual.

(7) 0 State. Opposite transistor in a binary conducting and indicates decimal weight absent.

(8) Truth Table. A table which lists the allowable 1 or 0 states of a system of binaries for each decimal digit to be represented. These states are listed in an order which presents the most significant digit first.

Example: In a 1248 code, binaries, D, C, B, and A are assigned decimal weights of 8, 4, 2, and 1 respectively. The decimal number 5 is represented by state 0101 and weights of 4 and 1 are present. BCD combinations for the digits 0 through 9 are listed in the truth table (table 8).

Table 8. BCD Decade Counting Unit Truth Table

D 8	C 4	B 2	A 1	Decimal
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
0	0	0	0	10=0

b. Timing and Signal Pulses. During a frequency measurement interval, there are several timing operations which occur in a particular sequence. The timing relation of several of the pulses to each other is shown in Figure 4. All the pulses are timed from the reset pulse. When the reset pulse occurs is a function of the display time control and a variable recycle time of up to ten seconds is possible. The reset pulse triggers the timing generator circuits which control the sequence of events required to make a measurement.

(1) Reset Pulse. The reset pulse serves to clear all circuits; that is sets the counter and divider circuits to a normal state and sets the ratio and control circuit and parity logic circuits for a counting interval. The trailing edge of the reset pulses serves to trigger the preset generator circuits.

(2) Preset Pulse. The preset pulse is developed by the preset generator circuits and serves to set preselected binaries in the counting unit to specific states.

(3) f-Frequency. The f-frequency is the unknown input frequency to be measured.

(4) f/N Frequency. The f/N frequency is the output frequency developed by the I.C. and S.C. circuits.

(5) f_2 Frequency. The f_2 frequency is a 1.5 KHz frequency generated in the F.S. circuit and serves as the slow time base signal.

(6) f_2N Frequency. The f_2N frequency is a function of frequency f applied to the I.S. circuit and the output from the F.S. circuit.

(7) * Four-N-Frequency. The 4N frequency is a burst of N developed in the ratio gate circuit from the ratio gate pulse and the f_2N signal.

(8) * N-Ratio Level. The N-Ratio level is a voltage applied to the I.C. circuit and serves to set the f/N signal ratio.

(9) * Ratio Gate Pulse. The ratio gate pulse applied to the ratio gate circuit serves to extract the N-signal from the f_2N signal to develop the 4N signal. The time of the 4N bursts is equal to $\frac{f_2/8}{2}$

(10) * Bursts of N Pulses. The bursts-of-N output pulses are developed from the 4N pulse train through the "B" logic.

(11) One-Megahertz Clock Frequency. The 1-MHz clock frequency is an accurate stable reference source for all timing functions.

(12) Read Pulse. The read pulse serves as an enabling pulse to transfer to the memory and readout circuit the N-Count data totalized in the counting units.

(13) Display Pulse. The display pulse, generated as a function of the stop binary being set provides an enabling pulse to the read one-shot flop-flop. (If an error reset is generated, the display pulse will gate it to the AD circuitry.)

(14) Error Reset Pulse. The error reset pulse triggers the reset circuit and causes a reset pulse to be generated when a consistency error is detected. After three (3) error resets the N-Ratio level will change.

(15) Alternate Reset Pulse. The alternate reset pulse resets the B logic circuit after a consistency error check is completed.

(16) Nine-Carry Pulse. The nine-carry pulse is developed in the time base counter. It occurs only when all decades reach a count of nine (9). This coincidence is used to trigger open and shut the N-Timing gate.

(17) Odd-Even Pulse. The odd-even pulse, gated with the parity enable pulse output, provides a trigger pulse to the error reset flip-flop if the B logic circuit final binary fails to reset to a reset state after two bursts-of-N

(18) A Reset Pulse. The A reset pulse resets the A logic circuit after a frequency measurement is made to assure the alternate reset flip-flop is reset.

(19) N-Timing Gate. The N-Timing gate pulse controls the counting time of the C.U. circuit. The pulse is developed in the ratio and control circuit and is called the count gate.

*Signals described in (7), (8), (9) and (10) are indicative of outputs with the range switch in the mid band position.

19. TYPICAL BASIC CIRCUITS

The following paragraphs describe basic circuits used in the frequency counters. Although the instrument is comprised of a number of individual printed circuit boards and associated wiring, its operation may best be understood by understanding the operation of the types of basic circuits used.

a. The Diode. Semiconductor diodes are used in signal-handling circuits and in power supply rectifier and regulator circuits.

b. The OR Gate. Two or more diodes are sometimes used as an OR gate. The OR gate is a multiple-input circuit which requires only one true* input condition to produce a true output condition. Figure 5A shows some OR gate configurations.

c. The AND Gate. The AND gate (or coincidence circuit) is a multiple-input circuit which requires the presence of all input signals in the true condition to produce a ture output condition. Figure 5B shows an AND gate configuration in which an input signal is passed only when properly polarized control voltages are applied.

d. The Inhibit Gate. An inhibit gate normally passes a signal. Adding a second signal closes the gate and prevents the signal from going through. One of the most common forms of the inhibit gate is the series gate shown in Figure 5C. If the diode is biased off, the gate is closed, and pulses do not reach the output. When the diode is biased on, the pulses pass through the gate and reach the output.

e. Limiter or Clipper. The limiter or clipper is a circuit which removes positive or negative peaks of waveforms. It can be used either as a waveform shaping circuit, or as a protective device to prevent excessive voltages from reaching a sensitive circuit. Figure 5D shows a limiter which prevents the negative peak or a pulse from going more negative than about -0.6 volt. Note that for a conducting silicon diode the cathode voltage is about 0.6 to 0.8 volt more negative than the anode.

f. Clamper or Dc Restorer. The clamper or dc restorer is a circuit which establishes either the positive or negative peak of a waveform at a particular dc reference voltage. This provides a definite base line voltage for the waveform. Figure 5E shows a clamper which provides a baseline of about +5 volts for a negative pulse.

g. Regulator. A diode regulator uses either the constant reverse-bias breakdown voltage characteristic of a breakdown (zener) diode or the constant forward-bias voltage drop characteristic of a semiconductor diode. Power supply reference voltages are generally provided by breakdown diodes which maintain a constant voltage when supplied with a reverse-bias voltage greater than their specified breakdown voltage. Regulated voltages can also be provided by a forward-biased diode which maintains a constant volt drop. Figure 5F shows connections for both types of diodes.

* True = "1" state = "set" state.

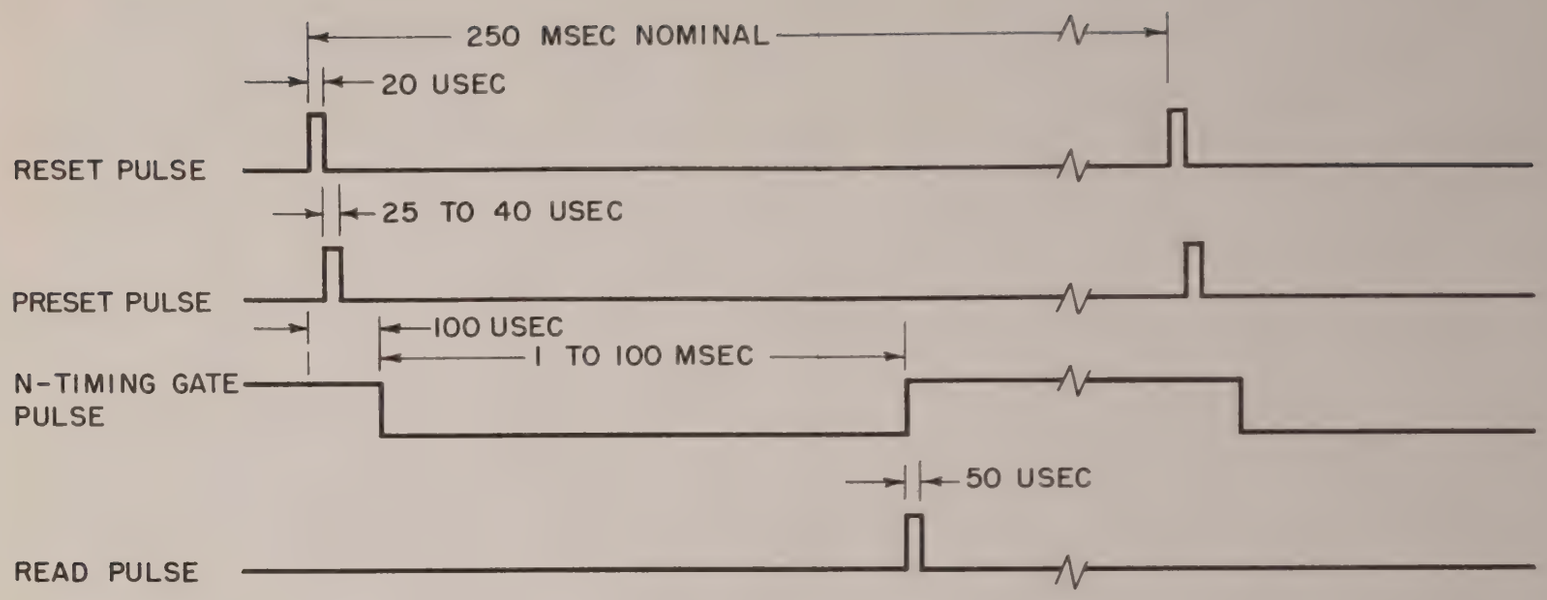
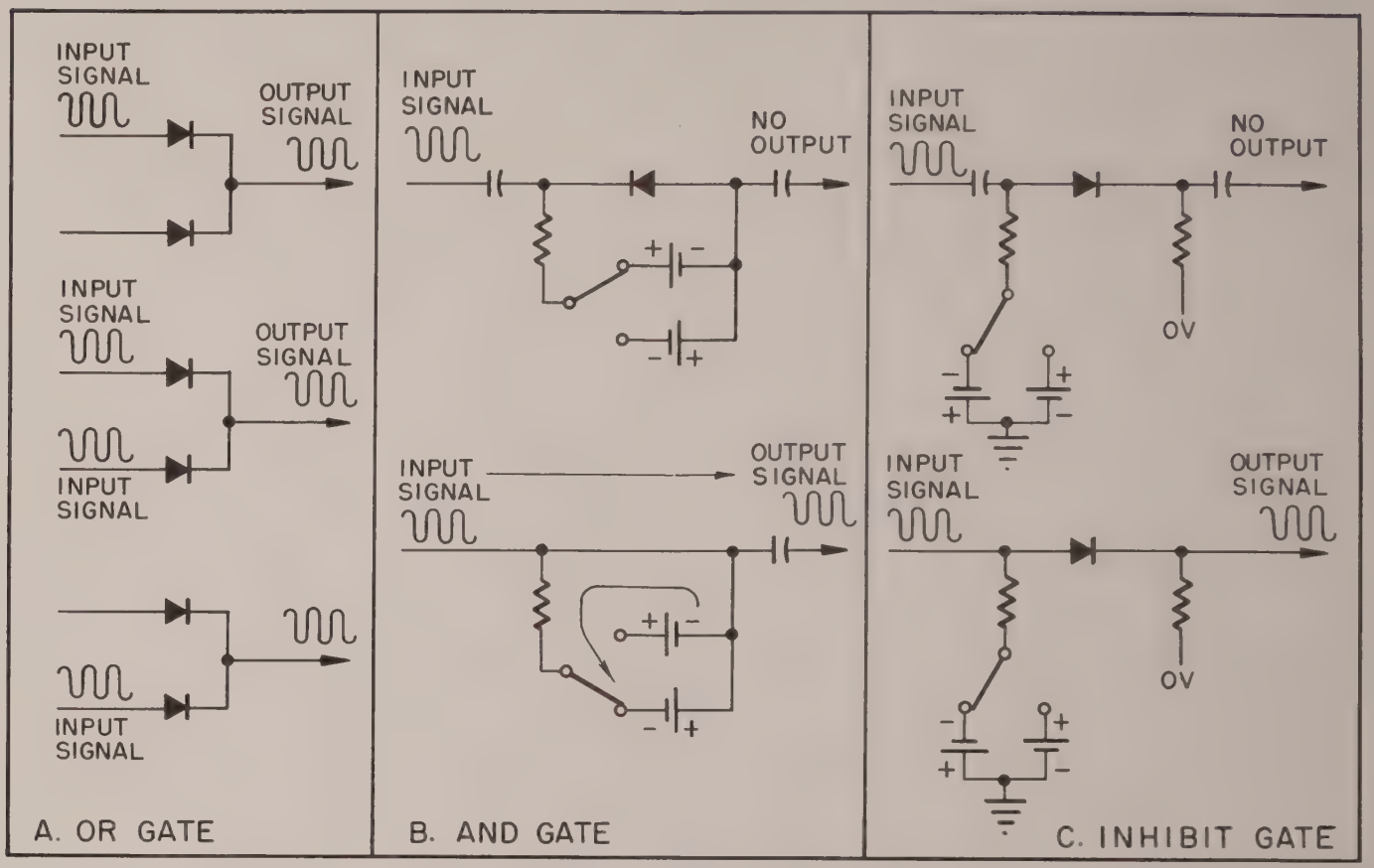


FIGURE 4. FREQUENCY COUNTER TIMING FUNCTIONS



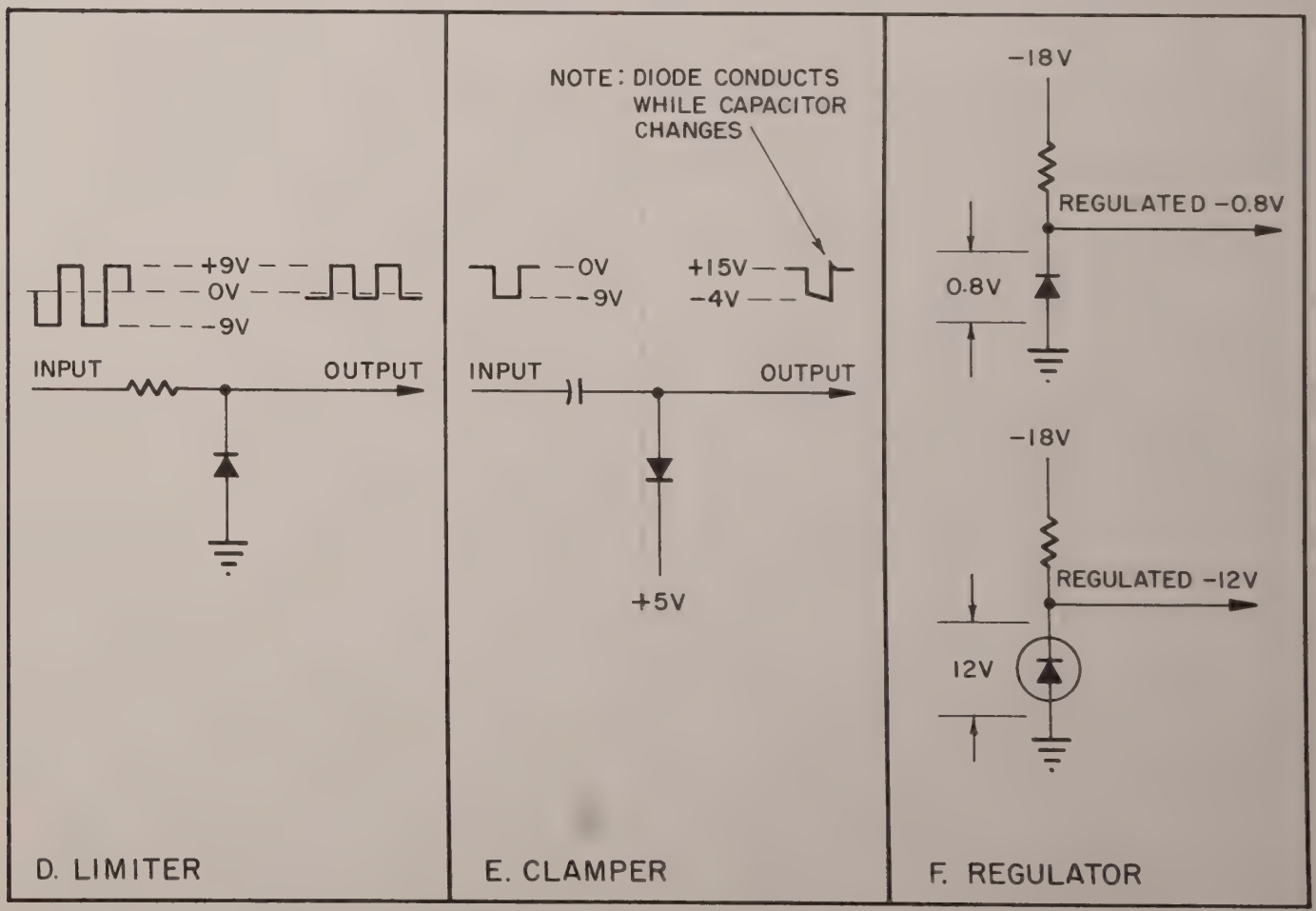


FIGURE 5. TYPICAL DIODE GATE CIRCUITS FUNCTIONS

h. The Transistor. Transistors are used throughout the frequency counter in circuit configurations such as the amplifier, the flip-flop or binary, the trigger circuit, and the one-shot multivibrator. In the following paragraphs, basic transistor operation and a few basic transistor circuits are discussed. These paragraphs discuss the easily observed changes in currents and voltages in transistor circuits which help technicians locate circuit faults but do not attempt to describe how transistors work internally.

i. Biasing and Conduction. Vacuum tubes and transistors are functionally similar. In the tube a small grid-to-cathode voltage controls a larger plate-to-cathode current flow. In a transistor a small base-to-emitter current controls a large collector-to-emitter current. A comparison of basic vacuum tube, NPN transistor operation is shown in Figure 6A. Notice that the effect of emitter-base-collector voltages is totally reversed between NPN and PNP transistors.

j. Amplifiers. As with vacuum tubes, three basic amplifier types are available (Figure 6B). These amplifiers may be used alone or in combination to form complex circuits.

k. Flip-Flop. The flip-flop is a bi-stable two-transistor circuit in which one transistor conducts, holding the other cut off. Each input pulse causes a reversal of states; that is the cut off transistor is turned on and the conducting transistor is cut off.

(1) In the flip-flop shown in Figure 7A, Q2 is initially conducting. A near-zero voltage is supplied to the base of Q1 from the R7 and R1 voltage divider. The ratio of the divider is such as to make the base voltage only slightly negative, to hold Q1 cut off. With Q1 cut off, the R6-R3-R2 divider delivers a negative voltage to the base of Q2 to keep it conducting.

(2) The flip-flop is initially set by a negative reset pulse applied to the base of transistor Q2. Diodes CR1 and through CR4 serve as steering and clamping diodes(steering diodes are to direct the positive input trigger to the on transistor turning it off). The input pulses are then applied to the bases of transistor Q1 and Q2 through capacitors C1 and C2 and steering diodes CR1 and CR3 which act as inhibit gates to the transistors. The reset pulse sets Q2 to conduct enabling the gate for Q2. The trigger pulses are differentiated by capacitors C1 and C2 to develop a negative and positive pulse. The pulses are applied through the steering diode that is enabled to the related transistor base.

(3) At time t_1 the positive input pulse cuts off Q2; the Q2 collector voltage goes negative and drives Q1 into conduction (R1-R7 divider to Q1 base); the Q1 collector voltage and the Q2 base voltage (R2-R3 divider) then become considerably less negative, holding Q2 cut off. In a similar manner the positive input pulse at time t_3 cuts off Q1 and a similar sequence of events takes place which ends with Q2 conducting and Q1 cut off. Note that a negative input pulse has no effect due to the steering diodes. This action continues as long as the input is available. A negative reset pulse applied to the base of Q2 returns the flip-flop to its initial conduction (Q2 conducting, Q1 cut off), this allows for synchronization of the flip-flop.

l. Binary Circuit. In this manual a flip-flop which completes its operating cycle and produces an output pulse after receipt of two similar input pulses is called a binary circuit. The binary circuit is driven from a single input which is connected either through a pair of resistors or through a pair of gating (steering) diodes to each transistor base.

m. Trigger Circuit. The trigger circuit is a squaring amplifier which produces an output waveform with very fast rise and fall times. Initially in the circuit shown in Figure 7B the input voltage is positive and Q1 is therefore cut off. The negative voltage applied to the base of Q2 through the R2-R3-R4 divider causes Q2 to conduct heavily. The input voltage (Q2 collector) is therefore only slightly negative.

(1) At time t_1 the input signal becomes sufficiently negative to drive Q1 into conduction. The voltage at the Q1 collector and the Q2 base (through the R3-R4 divider) becomes less negative and reduces the conduction of Q2, reducing the voltage drop across R5. The Q1 emitter-base forward bias increases to cause still heavier Q1 conduction. Action stops when Q1 is saturated and Q2 is cut off. Capacitor C1 bypasses R3 to couple fast changes in voltage at the Q1 collector to Q2 base.

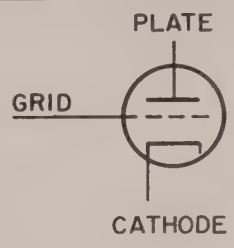
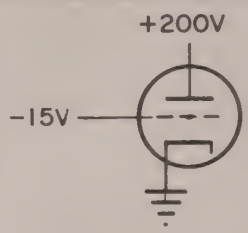
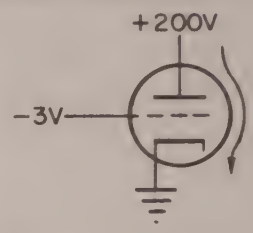
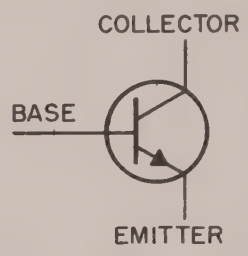
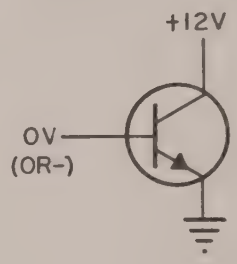
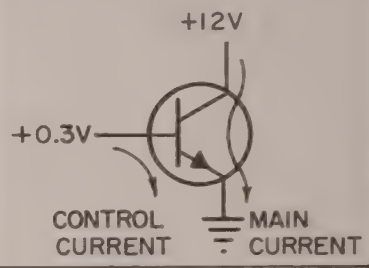
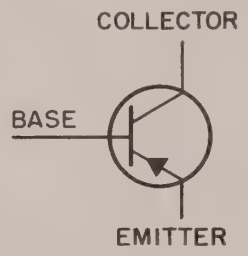
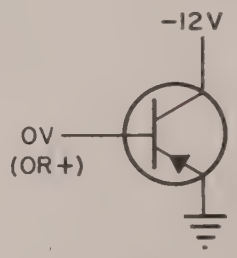
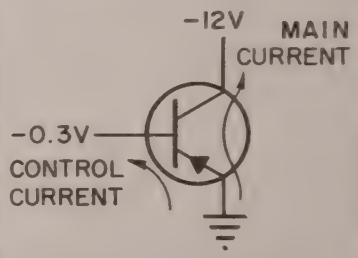
(2) At time t_2 the input voltage goes positive. Q1, conduction is reduced. Both the Q1 collector and the Q2 base voltage go negative and Q2 comes into conduction. Current flow increases in the R5, Q2, R1 voltage divider chain. Q1 goes into cut off, as the emitter-base forward bias is reduced.

n. One-Shot Multivibrator. The one-shot or monostable multivibrator is a circuit which generates a pulse of some specified duration following the application of a suitable triggering pulse.

(1) In the typical one-shot multivibrator shown in Figure 7C the following conditions exist during the initial stable period. The R1-R5 divider delivers a sufficiently negative potential to the base of Q1 to hold Q1 in saturation. The Q1 collector is therefore only slightly negative. The R2-R3-R4 divider delivers to the Q2 base a slightly positive voltage to hold Q2 cut off.

(2) The positive triggering pulse at time t_1 reduces conduction of Q1. The resulting negative-going voltage at the Q1 collector is applied to the Q2 base through the R2-R4 divider (C2 bypasses R4 to provide coupling for the rapidly changing voltage at the Q1 collector). Q2 begins to conduct. The resulting positive-going change in Q2 collector voltage is coupled through C3 to the Q1 base and further decreases Q1 conduction. The process is regenerative and quickly results in Q1 being cut off and Q2 being saturated.

A. TRANSISTOR BIASING

DEVICE	SYMBOL	CUTOFF	CONDUCTING
VACUUM TUBE			
NPN TRANSISTOR			
PNP TRANSISTOR			

B. AMPLIFIER CHARACTERISTICS

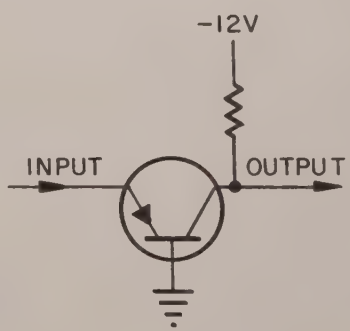
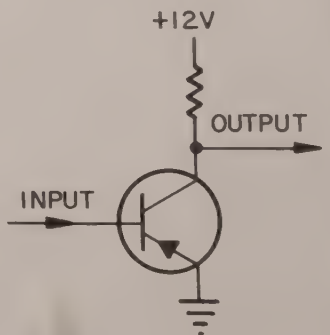
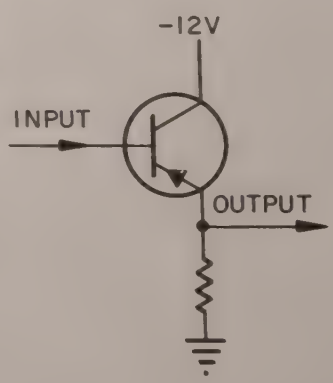
	COMMON BASE	COMMON EMITTER	COMMON COLLECTOR
INPUT Z	30-50 Ω	500-1500 Ω	20-500KΩ
OUTPUT Z	300-500KΩ	30-50KΩ	50-1000 Ω
VOLTAGE GAIN	500-1500	300-1000	<1
CURRENT GAIN	<1	25-50	25-50
POWER GAIN	20-30 db	25-40 db	10-20 db
			

FIGURE 6. TRANSISTOR OPERATION

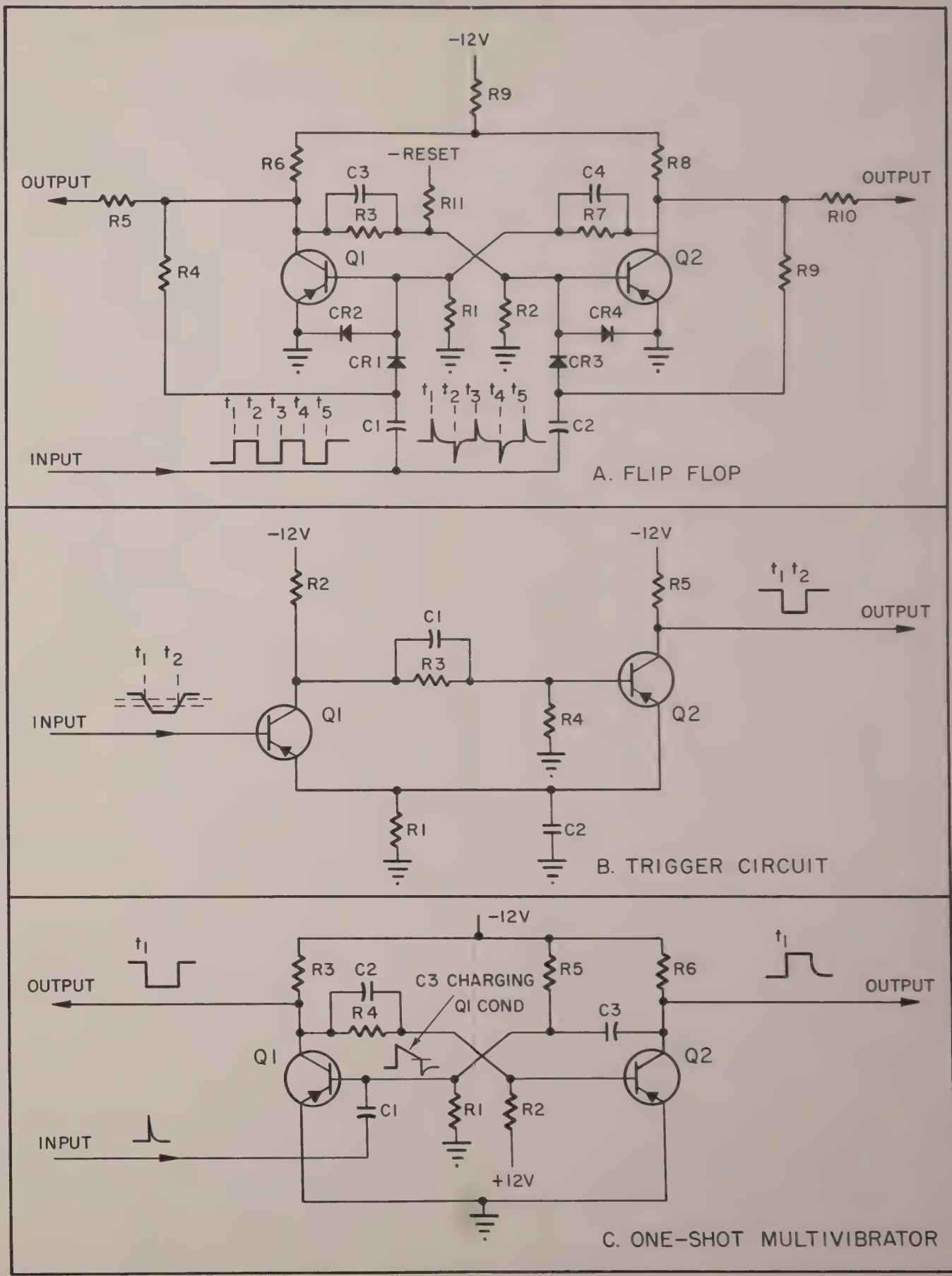


FIGURE 7. BASIC TRANSISTOR CIRCUITS

(3) Capacitor C3 now charges at a rate mainly determined by the values of R5 and C3. When the Q1 base voltage becomes sufficiently negative, Q1 begins conduction. The resulting positive-going Q1 collector voltage is coupled to the Q2 base. The Q2 collector voltage goes negative and is coupled through C3 to the Q1 base and further increases Q1 conduction. The process is regenerative and ends with the circuit in its original quiescent state (Q1 saturated and Q2 cut off).

o. Decade Counting Unit Basic Operation. The decade counting unit circuits are used to divide their input frequency by ten. Paragraphs 19 o (1) through 19 o (5) cover general operation of the counters with emphasis on counting logic, and Paragraphs 19 o (6) and 19 o (7) discuss associated readout circuits.

(1) Input and Output from Binary. Figures 8A and 8B show a flip-flop connected for operation as a binary circuit (basic flip-flop operation) and is discussed in Paragraph 21 k. Positive input pulses are applied to the bases of both transistors and causes switching by cutting off the conducting transistor. Negative reset pulses go to the base of one transistor and turn it on. Note the letter A near one transistor and $\overline{A}$ (read as "A bar" or "not A") near the other transistor. The positive-going transition at the collector of the A transistor (while switching from $\overline{A}$ conducting to A conducting) provides the input to the next binary circuit.

(2) Circuit Arrangement and Count Notation. Figure 8C is a block diagram of a typical four-binary decimal counter. Notice that the A output is applied to the B, $\overline{B}$ and D transistors and that the C output is applied only to the $\overline{D}$ transistor. Each input pulse produces a different combination of conducting and cut-off stages. There are only 10 allowable combinations and each combination represents a decimal digit. Decimal weighting is the decimal value assigned to the output of a pair when the plain-letter transistor is conducting.

(a) Decimal Count. Decimal weighting used in the decade counting unit (DCU) is shown in Figure 8C immediately above each of the four binary stages. The decimal weight each pair represents is present only when the plain-letter side (A, B, C, or D) is not conducting. When the barred-letter side ($\overline{A}$, $\overline{B}$, $\overline{C}$, or $\overline{D}$) is not conducting, the decimal weight is zero. The decimal count can be determined by adding the decimal weighting of the four stages.

(b) Binary-Coded Decimals. In binary-coded decimal notation, the output is either 1 (when the plain-letter transistor is not conducting) or 0 (when the barred-letter transistor is not conducting). In binary-coded decimal notation, the order of the binaries is given so that binary-coded decimals can be written with the least significant digit to the right. Thus, in the system used in the frequency counter the binary-coded decimal notation normally is

given in the order DCBA. (Decade counting unit binaries are shown in the ABCD order on the schematics and in Figure 8C to increase clarity in showing signal flow.)

(3) Sequence. Figure 8 shows the counting sequence for a typical decimal counter. Refer to 25-MHz decade counting unit schematic for circuit location of components herein referred. The 2.5 MHz and 250-KHz decade counting units circuits are similar except they do not contain the second gate circuit before the fourth binary. Initially after reset, each binary is in the 0 state (decimal count = 0, DCBA = 0000). The following action takes place when a series of input pulses are applied to the counter.

(a) The first pulse switches A binary to the 1 state (DCBA = 0001).

(b) The second pulse switches A binary to the 0 state. The output from a binary is applied through emitter follower Q10 to the AND gate input of B binary. Diode CR32 applies an enabling voltage to the AND gate. This permits diode CR8 to pass the output from A binary to switch the B binary to the 1 state (DCBA = 0010). The output of the B binary is AND gated with the A and C binaries (CR15, CR16 and CR23) to provide an input gate to the D binary.

(c) The third pulse switches A binary to the 1 state (DCBA = 0011).

(d) The fourth pulse switches A binary to the 0 state. The output from A binary switches B binary to the 0 state. The output from the B binary switches the C binary to the 1 state (DCBA = 0100).

(e) The fifth pulse switches A binary to the 1 state (DCBA = 0101).

(f) The sixth pulse switches A binary to the 0 state. The output from A binary switches B binary to the 1 state as in (b) above (DCBA = 0110).

(g) The seventh pulse switches A binary to the 1 state (DCBA = 0111).

(h) The eighth pulse switches A binary to the 0 state. The output from A binary switches B binary to the 0 state. The output from the B binary switches the C binary to the 0 state. The switching of the three binaries switches D binary to the 1 state (DCBA = 1000). Since the B binary input AND gate is enabled by the D binary, the switching of the D binary now inhibits the B binary gate, but, also enables part of the nine-carry gate function (CR30).

(i) The ninth pulse switches A binary to the 1 state. The output from A binary is applied to nine-carry AND gate through Diode CR31. This provides a pulse to the nine-carry line. Since nine-carry gate was enabled by the binary, the ninth pulse also causes an output pulse to occur from the nine-carry line (DCBA = 1001).

(j) The tenth pulse switches A to the 0 state. The output from A binary is applied as a gate ahead pulse to the D binary (through capacitor C18) and switches D binary to 0 state (DCBA = 0000).

(k) The switching of the D binary to 0 causes an output pulse to be generated by the decade counting unit which is applied to the next decade counting unit signifying ten pulses were counted.

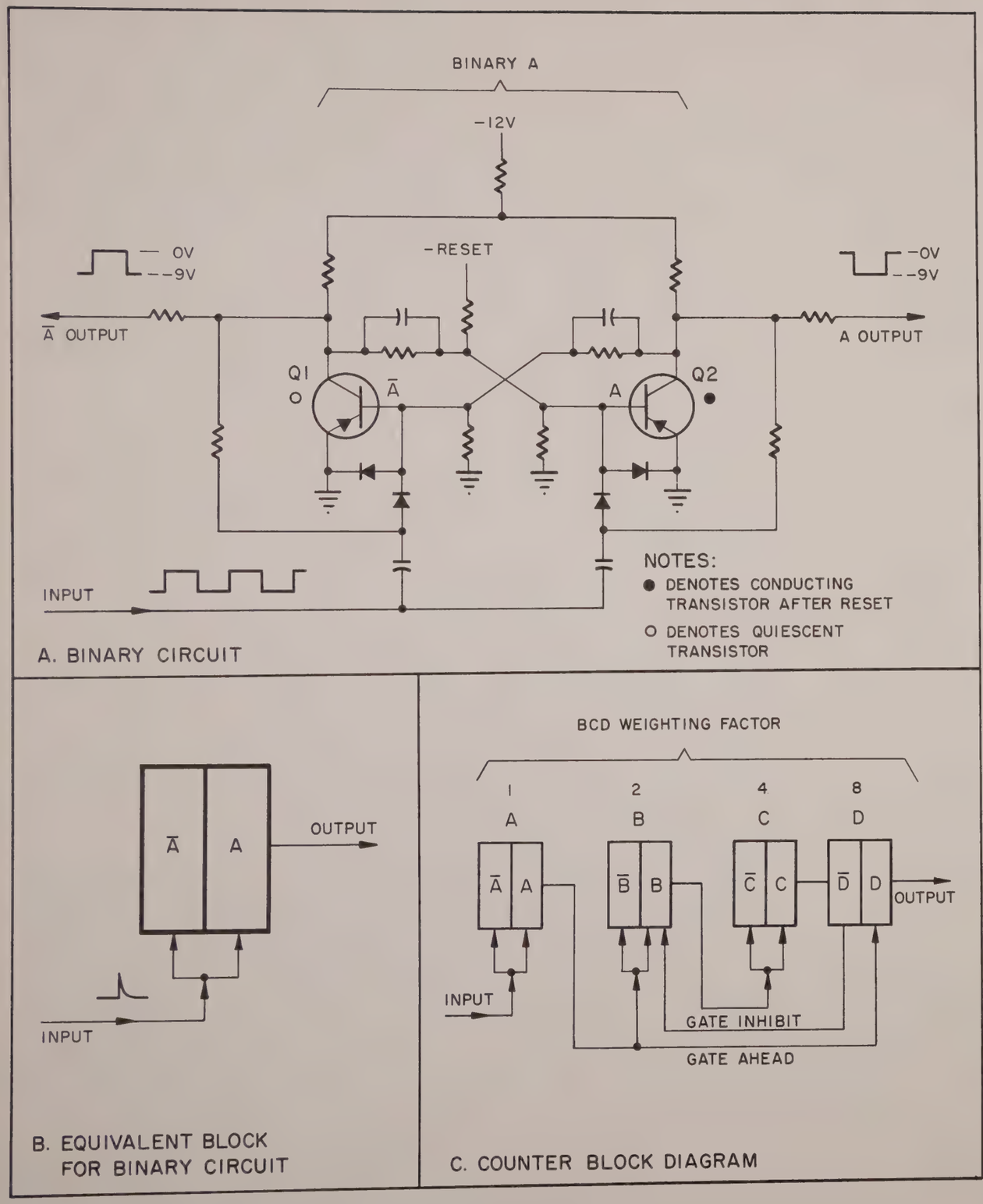
(4) Resetting to Zero. The reset pulse (negative) is applied to the base of the 1 state transistors (A, B, C, and D) in each binary circuit. If the 1 state transistor is not already conducting, this pulse will turn it on. In this manner the reset pulse ensures that all four 1 state transistors are conducting. Decade counting units can be reset as required to any desired state, since reset inputs are available at each transistor. Note the difference between a regular input pulse and a reset pulse: A regular input signal is positive-going and causes a conducting transistor to cut-off; a reset pulse is negative-going and causes a cut-off transistor to conduct.

(5) Timing. Waveforms showing time relationships for the binary counter are shown in Figure 8. Note that a driven binary switches only when the input wave is going positive.

(6) Electrical Readout. A four-line binary-coded-decimal output is available from the decade counting unit. A voltage representing the state of each binary is taken from the collector of each of the plain-lettered transistor (A, B, C and D). A binary 0 is represented by a relatively negative voltage (-9 volts) on each line. A binary 1 is represented by a relatively positive voltage (-0.3 volts) on each line. Table 7 summarizes the ten allowable combinations which represent the decimal digits 0 through 9. (To protect the binary circuit from being effected by the load, each output line contains a 6800 ohm series-connected resistor which is not located on the printed circuit board.)

(7) Digital Display. An associated matrix, containing a glow tube and associated decoding network, is used to convert the binary-coded representation to a decimal numerical representation. Refer to memory readout circuit, paragraph K for a discussion of decimal display functions.

(8) Presetting Count. A count preset circuit (containing a pulse generator and gating diodes) is used to set an offset count into the counters. The count can be any desired number as outlined in the specifications. The preset pulse functions in a similar manner as the reset pulse, except that it is applied only to the decade counting units in the counting chain. This pulse is only applied to the five most significant digits and the overflow lamps, in the 945/950 or the seven most significant digits in the 946/951. The readout in 0.1 MHz as called out in the specification applies only when the resolution switch is in position III.



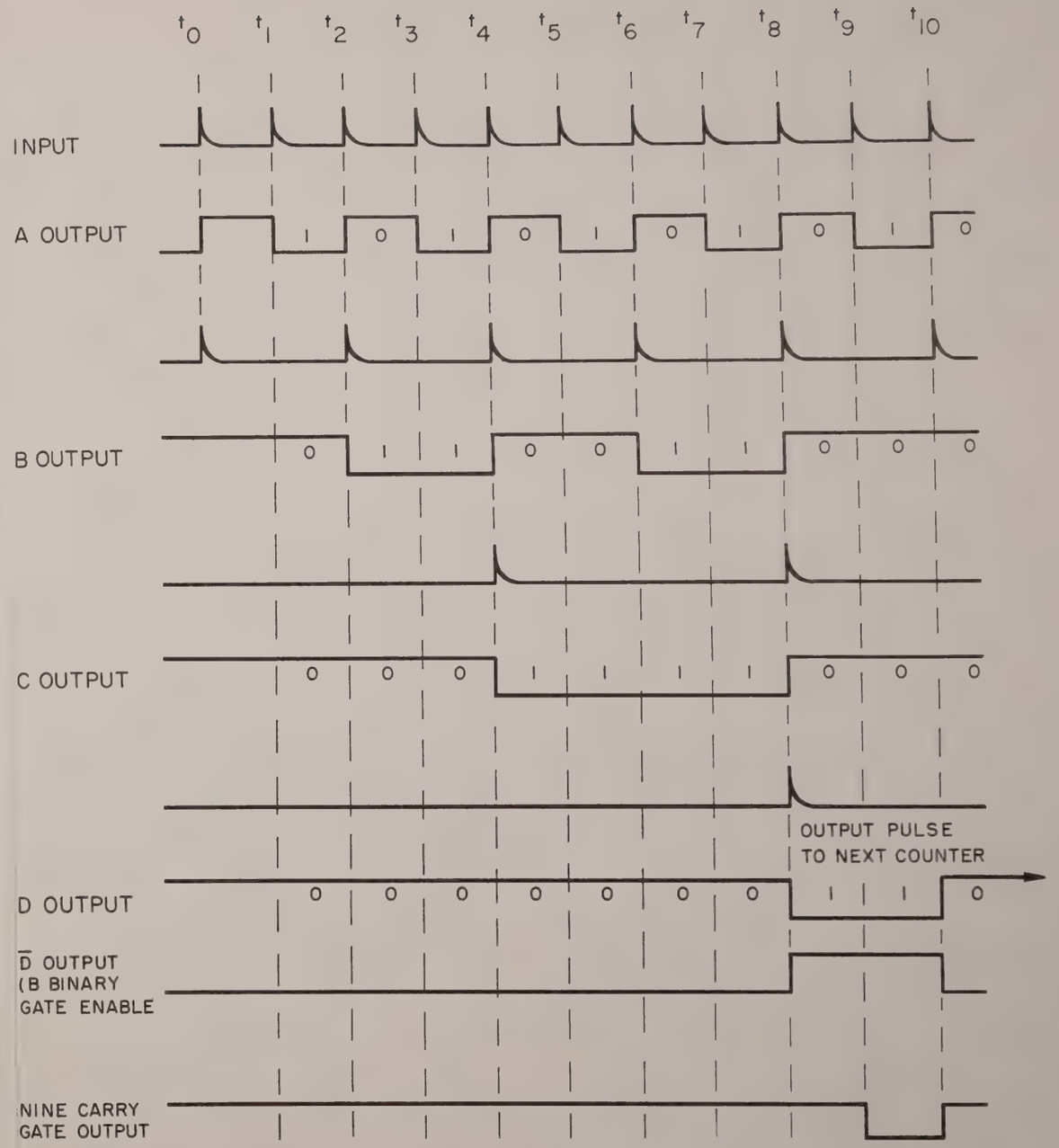


FIGURE 8. BASIC FOUR BINARY COUNTER AND TIMING FUNCTIONS

20. GENERAL

This section contains the principles of operation of the frequency counter circuits. Included is a simplified block diagram discussion and a detailed block diagram discussion for the circuit functions.

21. FREQUENCY MEASUREMENT TECHNIQUE

a. In the 900 series counters is found a new application for the familiar sampling technique, thus making possible for the first time direct digital frequency measurements in excess of 6 GHz. This use of sampling represents a significant advance in frequency counting offering distinct advantages over conventional counters. First, the direct counting bandwidth is increased by nearly two orders of magnitude. Second, frequency measurement time is greatly reduced as compared with conventional counters that employ heterodyne or transfer oscillator techniques, since such operations as tuning, nulling and calculating are eliminated.

b. The sampling technique is a process by which a lower frequency replica of a repetitive input waveform is produced by (1) measuring the input waveform amplitude for brief periods at selected points along the waveform and, (2) arranging these points to uniformly advance in phase. In this manner the entire cycle is ultimately covered with reasonable definition. The steady advance of the sampling points is called slewing. When the sampling technique method is applied to a frequency counter, it is only necessary to make a go-no-go decision as to whether the input signal is above or below the baseline reference point. That is, since the important factor is the counting of the frequency cycles and not in displaying a faithful replica of the waveform, the number of samples-per-cycle can be fewer than are required in sampling oscilloscopes. (See Figure 9.)

c. Many of the input circuits within the 900 series frequency counters are referenced throughout this manual as proprietary circuits. Complete detailed information is not revealed although input/output signals are described for trouble isolation. The schematics are included for basic servicing and for adjustment of certain specific controls. Specially constructed fixtures, special equipment and measurement techniques are required for overall servicing of the input proprietary modules. It cannot be over emphasized that component placement, lead dress, and even substitution of supposedly identical components can completely alter the operation of the circuit. Accordingly, servicing of the proprietary circuits should be limited to the adjustments described and to replacement of components only in those portions of the schematics which are shown.

d. The following description of the input circuits and sampling technique employed in the counters is greatly simplified and is included as an example of how the system functions. It should be understood that this is not an all inclusive explanation, but rather a guide to impart a basic understanding of the system. A complete description of all the circuitry in the proprietary modules would serve no useful function since servicing requires test fixtures and equipment available only at the factory.

(1) Figure A is a block diagram of a simplified frequency counter.

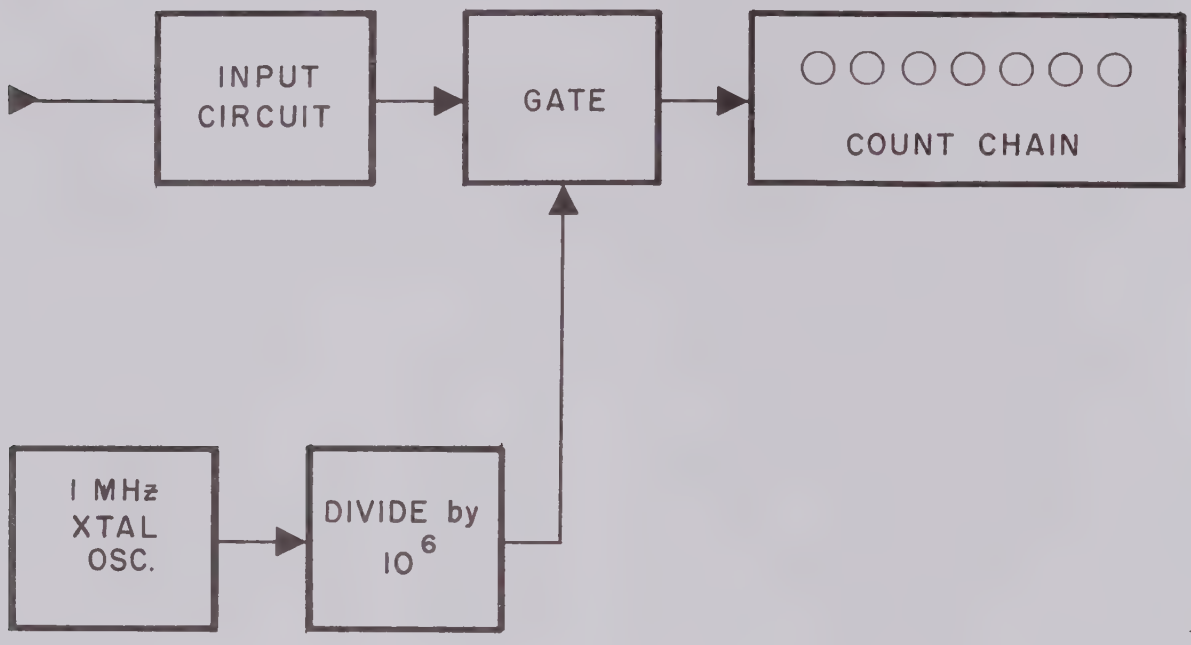


Figure A. Conventional Frequency Counter Simplified Block Diagram.

(a) The input circuit amplifies or attenuates the input signal as required and applies the processed signal through a gate to a count chain. The gate is opened by the time base for one second. The visual presentation on the count chain is how many events have occurred in one second - or events per second. Obviously, a frequency counter has additional circuitry to provide variable display time; perhaps time bases of other than one second to provide different resolution and many conveniences features.

(b) The Models 945 and 950 are quite similar. In fact, the low band (20 hertz to 100 megahertz) works precisely as described above and uses a time base of 0.1 second, to provide a resolution of 10 hertz. Where these instruments differ from the conventional counter is in the mid and high bands. Here the series uses a sampling technique - previously found only in certain oscilloscopes.

ORIGINAL

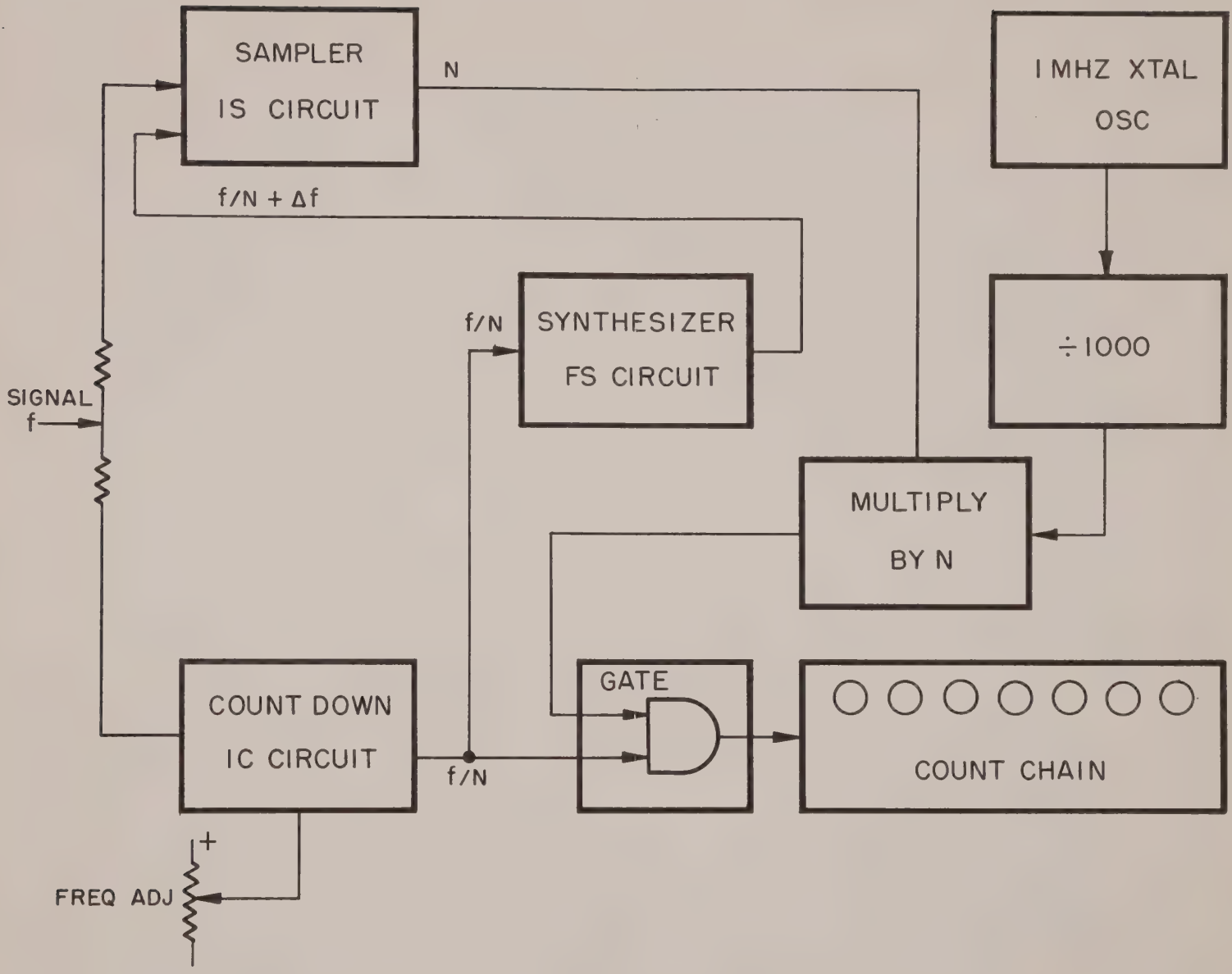


FIGURE 9. SAMPLER COUNTER, BLOCK DIAGRAM

(2) The purpose of the sampling technique is to reduce the input frequency to enable ordinary counter circuits to count very high frequencies. The following very simplified explanation is provided to give an overall systems view of the 900 series. The explanation is specifically for the mid band but applies, other than for some of the frequencies mentioned, to the high band as well. Also, the discussion is limited to the Models 945 and 950 of the series since they are simplest while the techniques are common to the entire series.

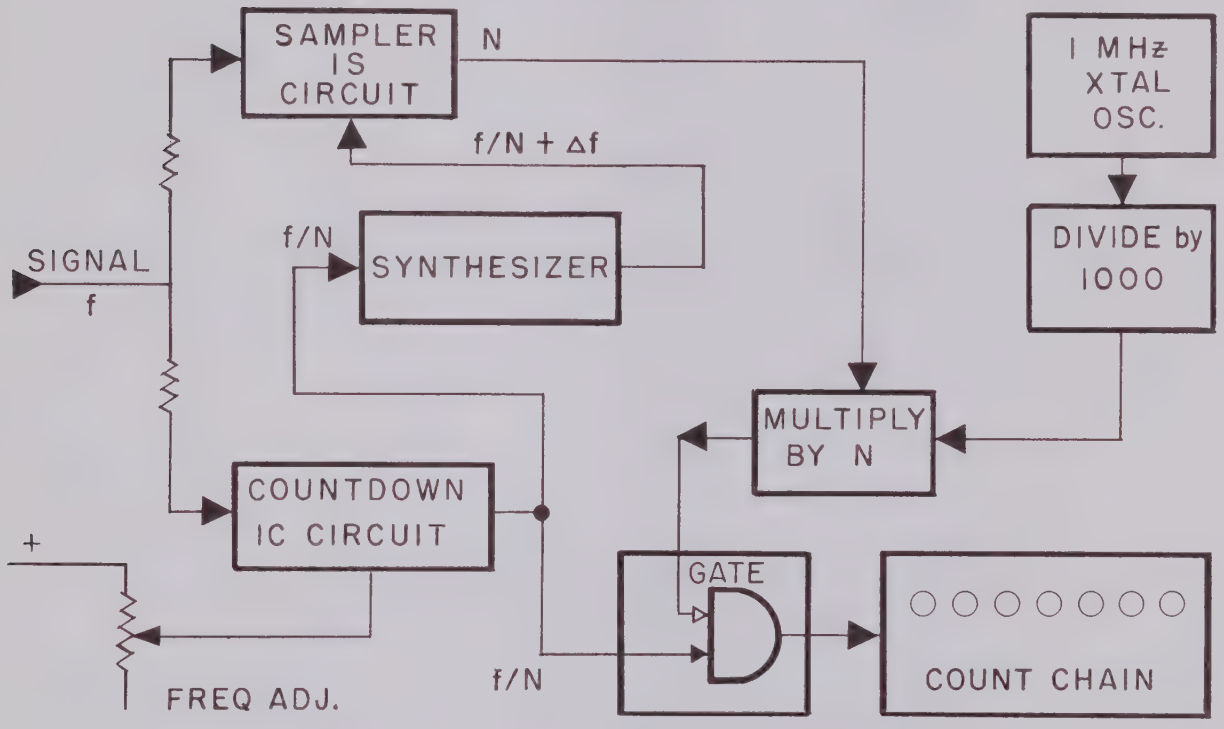
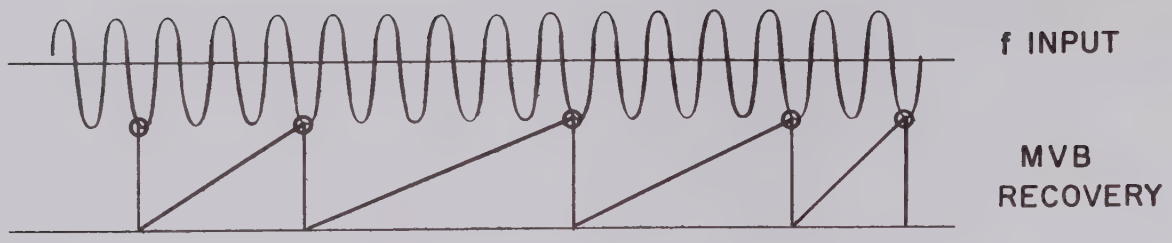
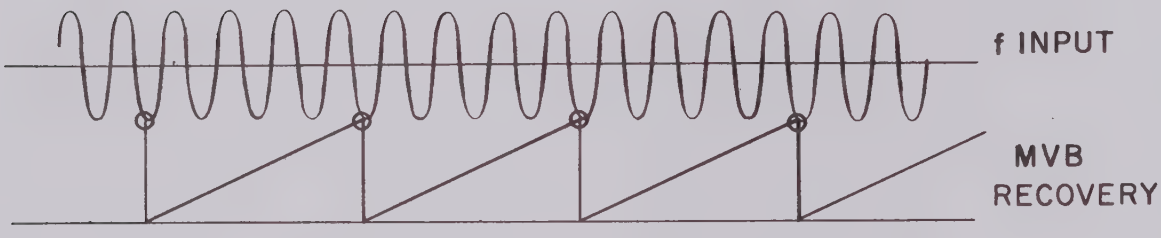


Figure B. Input Sampling Circuit Simplified Block Diagram.

(a) The countdown (IC circuit) is an astable multivibrator (MVB) which has the ability to trigger back and forth at a natural rate of about 10 megahertz. This natural frequency can be varied slightly (from approximately 9 to 10 megahertz) by a DC bias adjustment. An input signal higher than this natural frequency can drive the multivibrator at some sub-multiple of the input frequency. A slight variation of the DC bias may be required to permit stable division, as illustrated in Figure C.



Unstable



Stable

Figure C. Astable MVB Output Adjusted For Stable Operation.

In other words, the output frequency will be some sub-multiple of the input frequency and the output is f input divided by N or f/N as we will use in further explanation.

(b) To determine the input frequency, the output frequency of the countdown can be measured on a conventional counter and the result multiplied by N. The only remaining problem is to determine the frequency division which has occurred - in other words, to determine the value of N. This will be the function of the input sampler (IS circuit).

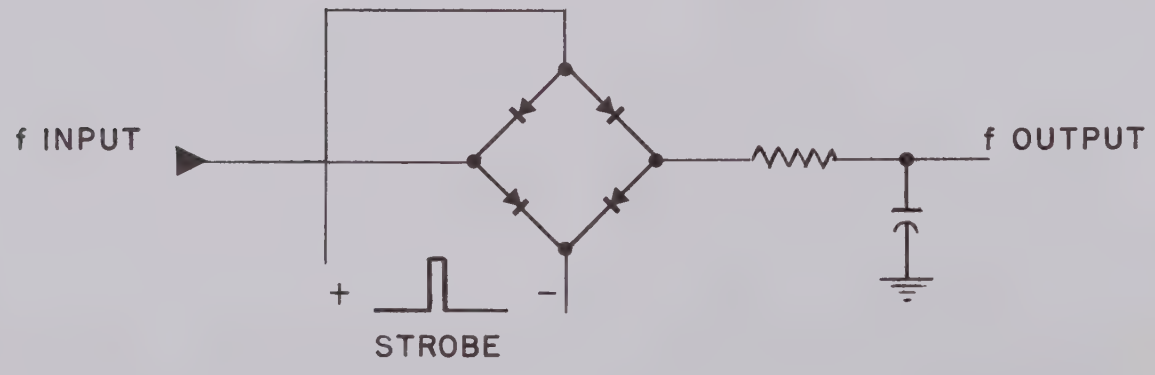


Figure D. Simplified Input Sampler Circuit.

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Suppose we sample f input at the output rate of the countdown (IC circuit). Assuming the countdown is syncronized to a sub-multiple, - say 1/4 of the input frequency - the strobe pulses (which occur at the count-down rate) would permit the input bridge to conduct at a certain point of the cycle of f input. Since the ratio of the two frequencies does not change (they are syncronized) the sample occurs on the same part of the input wave form each time. The output of the sampling bridge is therefore only a dc level proportional to the amplitude at the point on the input waveform at which sampling occurs. Unfortunately, there is no information here to be used in the determination of N.

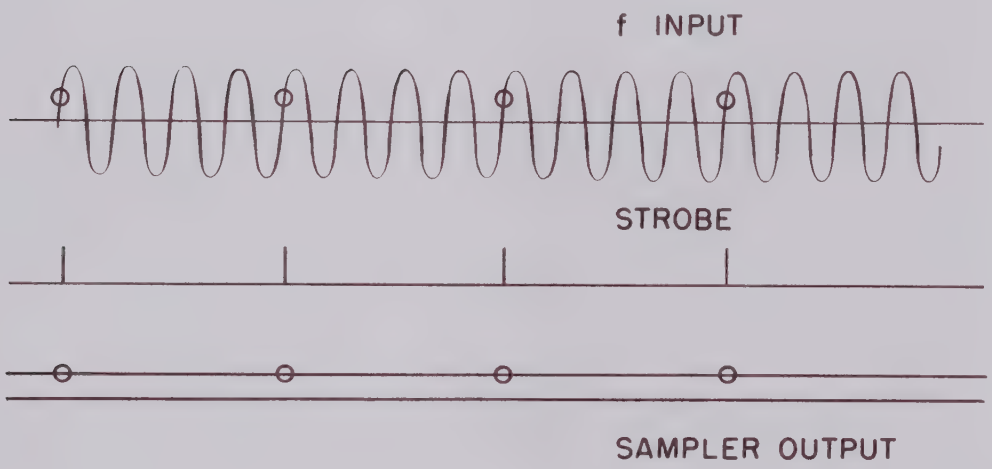

Figure E. Sampler Output Without Slewing.

If the sampling frequency were slewed (each sample occurring slightly later or sooner in time) each successive sample would occur on different points of the input waveform.

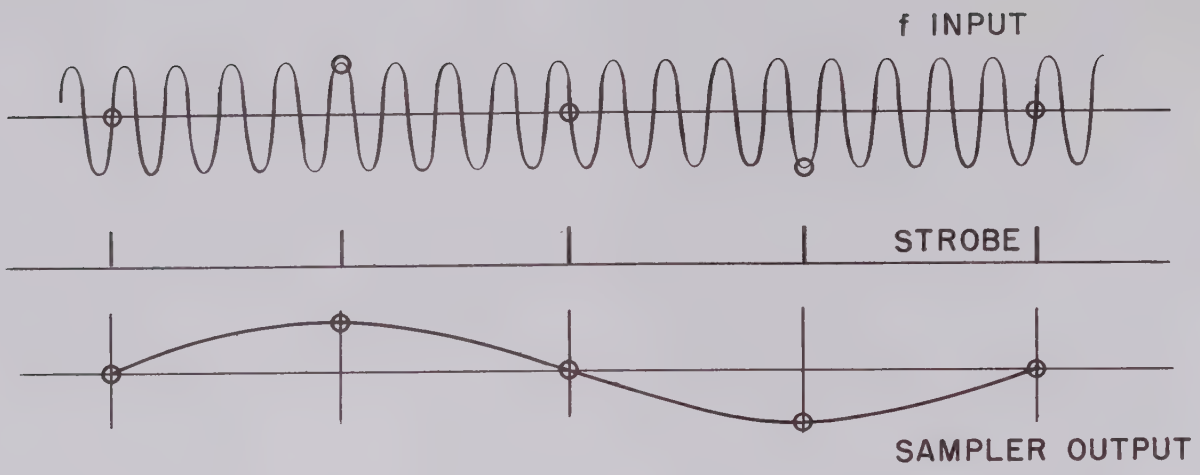

Figure F. Sampler Output With Slewing.

(c) The sampler output is now a lower frequency reproduction of the input frequency. In the example shown, the sampler output is 1/16 of the input frequency. The slewing of the sampling strobe pulses is accomplished by the frequency synthesizer (FS circuit):

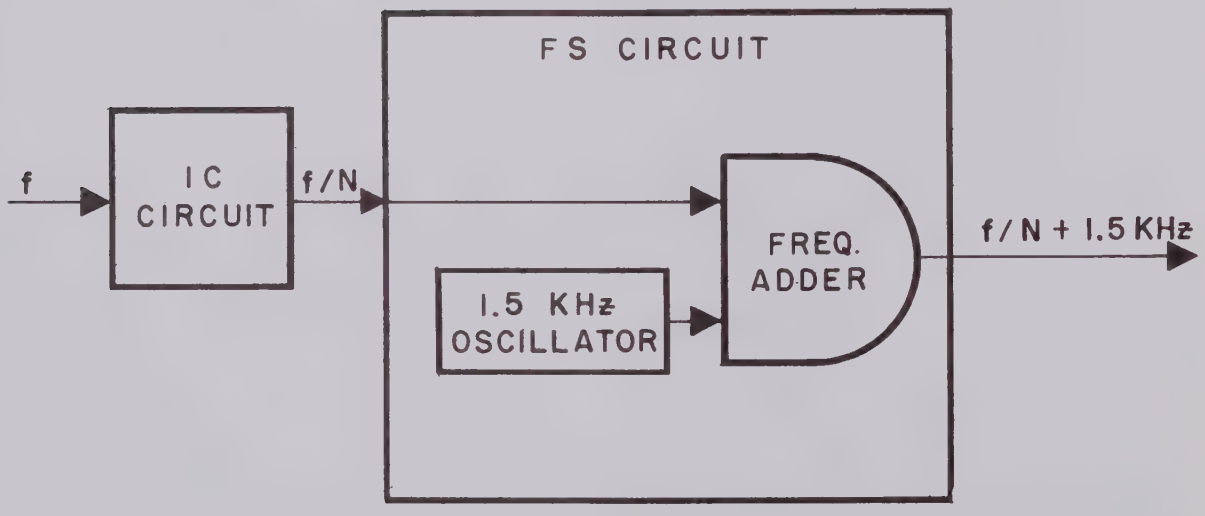

Figure G. f/N + 1.5 KHz Output Simplified Logic Diagram.

The output from the countdown (IC circuit) has added to it a frequency of approximately 1.5 kilohertz (Δf) in the synthesizer. Since the countdown output is some fixed sub-multiple of the input frequency, the output of the synthesizer is:

$$f/N + \Delta f$$

The addition that is performed can be shown by two vectors: Vector f/N and Vector Δf.

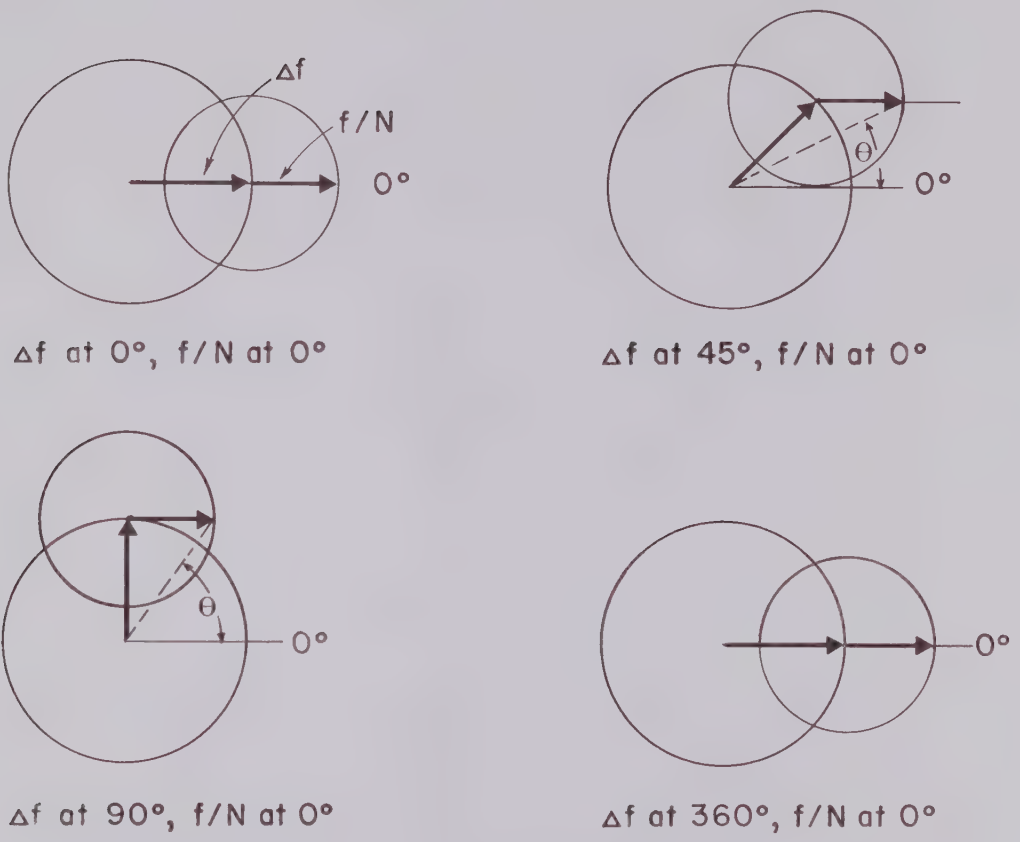

Figure H. Vector Addition of f/N and Δf.

The two vectors rotate in a counter clockwise direction at a rate determined by the respective frequencies. In the examples shown, are pictured the resultant (dotted vector) at the time when the f/N Vector is at 0°. The resultant is shown to be a progressive phase change as the Δf vector rotates through 360°. In other words, in respect to the original 0° reference, we have progressively advanced the point of initial reference of the f/N vector through 360° as the Δf vector makes one revolution. Note that at the completion of one revolution of Δf we are back to the initial starting point with both vectors at the 0° reference point.

To keep the numbers simple, assume a countdown (IC circuit) output frequency of exactly 10 megahertz. Therefore, f/N = 10 MHz. For further simplicity, assume a Δf of exactly 1 kilohertz. In the vector representation then, the Δf vector makes 1,000 counter clockwise revolutions per second, while the f/N vector makes 10,000,000 revolutions per second. Therefore, the Δf vector makes 1 revolution in one millisecond and the f/N vector makes 1 revolution in 100 nanoseconds. Our concern is with the f/N vector since this is the frequency which must be slewed for the sampler. We have shown that the resultant phase of the f/N vector changes 360° for 1 revolution of the Δf vector. In other words, since 360° of the f/N vector is 100 nanoseconds, we have made a total change of 100 nanoseconds in one millisecond (the period of the revolution for the Δf vector). The problem then becomes: how much change occurs in the time of f/N passing the initial zero reference over a period of 100 nanoseconds of Δf, if 100 nanoseconds of change occurs in one complete period of one millisecond of Δf? Thus:

$$\frac{\text{X change}}{100 \text{ nsec}} = \frac{100 \text{ ns}}{1 \text{ millisec}}$$

$$\text{X change} = \frac{10^{-7} \cdot 10^{-7}}{10^{-3}} = 10^{-11} \text{ sec} = 10 \text{ picosec}$$

The slewing rate, per period of f/N is 10 picoseconds. Each 100 nanosecond period of f/N loses an additional 10 picoseconds. Since we use the f/N + Δf signal from the synthesizer (FS circuit) to strobe the sampler, each successive sample will occur 100 nanosec minus 10 picoseconds sooner than the previous. Thus, if the first sample is at 100 nanoseconds (100,000 picosec) the next would occur 100,000-10 picoseconds later, or at 100000, 199990, 299980, etc., picoseconds respectively.

Another way of looking at our vectors is to note that in one revolution of Δf, we have advanced the phase of f/N by 360°. Since 360° is one cycle, in each cycle of Δf we have added precisely one cycle of f/N.

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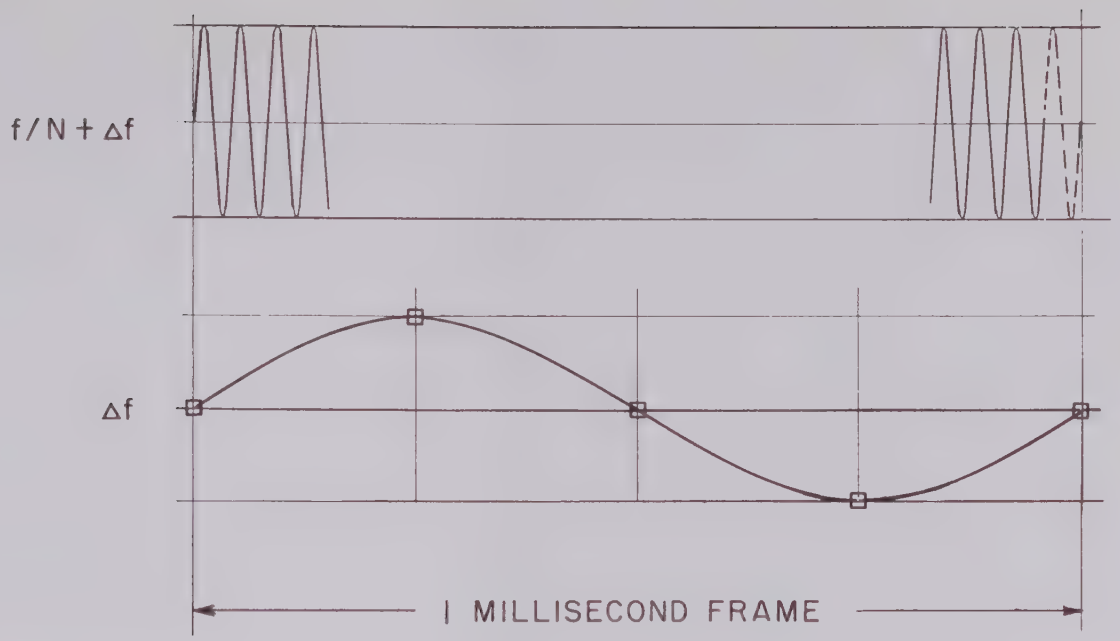

Figure I. Addition of f/N and Δf.

If f/N equals 10 megahertz, 10,000 cycles will occur in a millisecond frame of one cycle of Δf. Since Δf adds one cycle, 10,001 cycles of f/N + Δf occur within the frame. This corresponds to a time per cycle of f/N of:

$$100 \text{ nsec} \left(\frac{10,000}{10,001}\right) = 99.990000999900 \text{ nsec.}$$

The slew rate (change in time per cycle) is therefore approximately 100-99.9900 = 0.010 nsec = 10 picosec. Our slew rate is approximately 10 picosec per cycle

or exactly $10 \left(\frac{10,000}{10,001}\right)$ picosec per cycle.

(d) Now let's sample an input signal: Assume, for simplicity, an input frequency f of 500 megahertz and for further simplicity a countdown output (f/N) of 10 megahertz, a slewing frequency (Δf) of 1 kilohertz and a slew time of 10 picoseconds.

The period of 500 megahertz f is 2 nanoseconds. In a 1 millisecond frame 500,000 cycles of f will occur. Similarily, 10,000 cycles of f/N will occur and, because we add precisely one cycle of f/N with Δf, 10,001 cycles of (f/N + Δf) will occur. Since (f/N + Δf) performs the strobing of the input f, 10,001 sampling strobes will be performed.

The sampling slewing rate is 10 picoseconds per cycle. In order to progress entirely over and sample an entire cycle of the input frequency f, which has a period of 2 Ns or 2,000 picoseconds, 2,000 ÷ 10 or 200 strobes must be performed. In other words, one low frequency replica of the input f will be produced after 200 samples. In a time frame of 1 millisecond where a total of 10,001 strobes occur, 10,001 ÷ 200 cycles of the reproduced input will occur; or 50.005 cycles.

The answer obtained is slightly high because of approximating the slew time as 10 picoseconds. The actual slew time is $10 \left(\frac{10000}{10001}\right)$ picoseconds.

Therefore the answer is high by the factor of $\frac{10,001}{10,000}$
Our correct answer is thus: $50.005 \left(\frac{10,000}{10,001}\right) = 50.000$ cycles.

The output of the sampler is the N in f/N. In our example where f/N = 10 MHz and N = 50, f = 500 MHz.

Note that the exact frequency of Δf is not critical as long as the sampler output (N) is referenced to the Δf time frame. In the 900 series the Δf frequency is actually something between 1.5 to 1.6 KHz (a time frame of approximately 650 microseconds) and is identified as f_2 throughout the manual.

The referencing of N to the time frame of Δf is performed in the Ratio Gate circuitry.

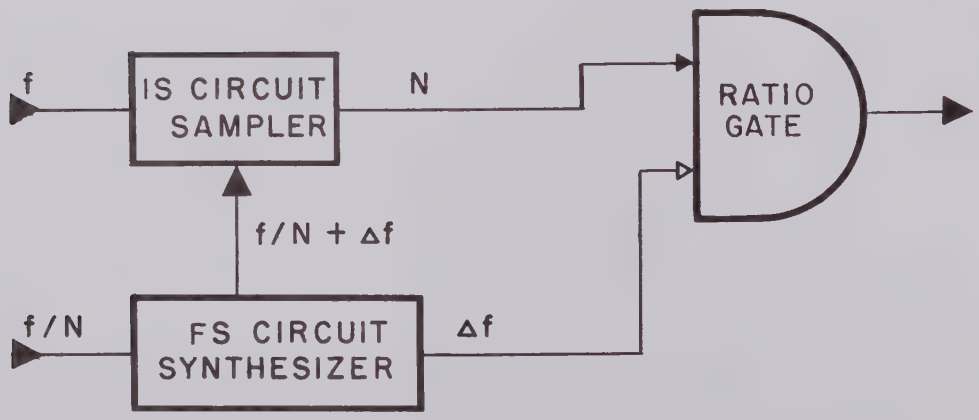

Figure J. N Gating Simplified Block Logic.

The output of the Ratio Gate is cycles of N per cycle of Δf. The cycles of N are used to preset two decimal counting units in the time base count chain to perform the necessary time base multiplication.

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A correct measurement cannot be made by the counter until the N number is set into the time base. One way to accomplish this would be to put the Δf frequency through a binary. With the output of the binary controlling the counter, the first cycle could be used to set the value of N and the next cycle used to permit the counter to measure f/N as multiplied by the value of N. In the 900 series the actual measurement is delayed even more by the parity circuit where successive values of N are checked for consistency. The operation of the parity circuitry is described in detail in paragraph 22 C, and also in Section III.

22. SIMPLIFIED BLOCK DIAGRAM

The frequency counter circuits are arranged in six basic circuit functions. The input circuits, the 1-MHz clock circuits, the time base generator circuits, the preset circuits, the parity check circuits, and the counting unit. The range selector switch, not outlined in the block, determines the operating mode of the instrument.

a. Input Circuits. The input sampler unit consists of the input power divider assembly, the I.C. circuit, the S.C. circuit, the F.S. circuit, and the I.S. circuit (see Figure 10). The power divider routes the frequency counter input signals to the input sampler unit circuits.

(1) The input signal is routed through the power divider to the I.C. and I.S. circuits. In the low band the input is coupled directly to the C.U. circuit in the counting unit. The low band does not employ the sampling technique.

(2) The input frequency and the N-Ratio level voltage, generated by the ramp generator circuit are applied to the I.C. circuit. The I.C. circuit processes the two signals to develop the signal ratio of f/N. This f/N signal is applied to the S.C. circuit for further processing producing the f/N signal at its outputs. The f/N signal (N-Count) is then applied to the F.S. circuit and the C.U. circuit. Also supplied to the C.U. circuit is the N-Timing gate. Due to the control action of the N-Ratio level voltage applied to the I.C. circuit, the f/N signal will be a continuous signal that is a ratio to the f-input frequency and will always be between 9 to 10 megahertz.

(3) The F.S. circuit generates a short time base signal f_2 (frequency 1.5 KHz) and also after further processing of the f/N signal (supplied from the S.C. circuit) applies the $f/N + f_2$ signal to the I.S. circuit.

(4) The input f-frequency, supplied from the power divider, is processed in the I.S. circuit with the signal supplied from the F.S. circuit to develop the f_2N signal. The f_2N signal is a continuous signal which is then applied to the ratio gate circuits with the ratio gate pulses for processing.

b. Time Base Generator Circuit. The time base generator circuit for the seven digit instruments as described herein is referenced to the 1-MHz crystal oscillator (see Figure 10 and 13) and serves as the time referenced for all timing functions (see Figure 12). The time base generator circuit consists of, the 1 MHz crystal oscillator, the time base delay circuits, the divide by 1000 and divide by 100 time base count chain (made up of five DCU's), the ratio and control circuit also referred to as the RC circuit), the ratio counter chain (two DCU's), the A logic, the ratio gate, the B logic and the reset circuit. The 1-MHz oscillator output frequency is divided down through three decade counters to develop a precision 1-KHz pulse output. The 1-KHz pulse output is applied to two additional decade counters to develop a 10 hertz pulse. The nine-carry function

from the five decade counters and AND'ed together and applied as a trigger pulse to the start-stop flip-flop circuits (N-Timing gate) of the ratio and control circuit. The N-Timing gate pulse width, developed by the time base (count chain) generator circuit, is controlled by the ratio counter chain. Since the N-Timing gate pulse width is a function of the N-Ratio (determined by the I. S. circuit) and the frequency being measured, the time base pulse width will vary for different frequencies. The A logic, the ratio gate circuit and the B logic processes the f_2 and f_2N signal to help produce the N-Ratio. The reset circuit provide the necessary reset signals to produce a common condition throughout the instrument. Circuit synchronization originates at reset time. In the nine-digit instruments a resolution switch and two additional decade counting units are added to the time base generator circuits. The time base count chain in the seven-digit instrument is in two sections (five DCU's total) a divide by 1000 section and a divide by 100 section. In the nine-digit instrument two sections (seven DCU's total) are used but the amount of division changes. The resolution switch provides for the first section to divide by 100, 000 in position IV, by 10, 000 in position III, by 1, 000 in position II and by 100 in position I. The second section remains unchanged fixed at a division by 100. As an example in the seven-digit instrument the output repetition rate of the first section is 1 KHz; a nine-digit instrument will have an output repetition rate at this point related to the setting of the resolution switch. In position IV the repetition rate will be .01 KHz, in position III .1 KHz, in position II 1 KHz and position I 10 KHz.

c. Parity Consistency Check. The parity logic circuit monitors the frequency measurement, performing consistency checks of the frequency counter computation circuits. The parity circuits consist of the P logic (parity), the A.D. and divide by 16 circuit, the divide by 8 circuit, the R generator (ramp) circuit and the gate centering circuit. Several successive N numbers are compared, the number of comparisons being determined by the setting of the front panel PARITY control. A go-no-go condition is detected by the parity circuits and the N number is transferred to the display indicators or an error reset is produced and the indicators read all zeros.

(1) The purpose of the parity check is to inhibit false measurements, therefore "Error Reset" will occur only during false measurements and no such signal will occur during accurate measurements. If the frequency measurement consistency check comparisons are dissimilar (caused for example by noise or the signal source frequency changing as it is being counted) the results of the confidence check will signify a consistency error and an error reset pulse will be generated. The error reset pulse, is applied to the reset circuit, the A.D. circuit, and the memory readout circuit. This will cause the display to show either all zeros or a preset number as previously described. If the signal source output is normal (within the operating range of the channel selected) continuous display of all zero's or the preset number is indicative of a malfunctioning frequency counter. All zero's or the preset number will be displayed until the parity circuit determines that a consistent frequency measurement is accomplished and no error pulses are generated.

(2) The A.D. circuit develops a trigger pulse that is applied to the ramp generator circuits. If three error reset pulses are successively generated, the A.D. circuit generates a pulse to cause the ramp generator circuit to step to a new N-Ratio level. The N-Ratio level, applied to the I.C. circuit, causes the I.C. circuit to change to a new ratio.

(3) A greater-than-90 signal (indicating a frequency beyond the range selected) serves to reject frequency ratios greater than 90 by producing an error reset signal. The frequency counter is designed

to measure reasonably pure sinusoidal continuous wave signals. Although a distorted signal rich in harmonics may be measured, it may cause frequent consistency error indications and may display the harmonic frequency instead of the fundamental frequency. The greater-than-90 circuit is designed such that an error reset signal will be produced each time the ratio counter counts to 90 during parity enable time.

d. Preset Selection. Prior to accumulating an N-count, the preset generator (located on the time base delay board) produces a preset pulse. This sets a predetermined preset number into the counting unit. This signal is generated by a trailing edge of the reset pulse. The preset reset thus is essentially subtracted from the incoming N-count.

e. Counter Circuits. The decimal counting circuit consists of a C.U. circuit, a matrix circuit, six decade counting unit circuits and seven memory readout circuits (see Figure 13). The f/N signal (generated in the S.C. circuit) is applied to the C.U. circuit and is counted for the duration of the N-Timing gate. (The N-Timing gate is supplied from the time base generator ratio and control circuits.) The states of the C.U. circuit and the decade counting unit circuits are applied to the memory readout circuits for final decimal display.

(1) The C.U. circuit is a high-speed counter circuit which divides the input N-Count by ten and supplies an output to the six other decade counting units for accumulating. In the nine digit instruments the C.U. circuit drives eight decade counting units. The C.U. circuit final-count states are applied to a memory readout circuit through a matrix circuit decoder.

(2) The matrix circuit amplifies the C.U. circuit final count states and also converts the bi-quinary code to a binary coded-decimal code (BCD) through a decoder circuit. The BCD code is then applied to a memory readout circuit for display.

(3) The one tenth of N-Count (CU circuit output) is accumulated by the decade counting units which serve as binary-coded-decimal dividers. The input pulses are divided down by ten in each DCU during the enabling interval of the N-Timing gate. The closing of the N-Timing gate (by the stop flip-flop) stops the accumulating function. At this time display and read pulses are generated.

(4) The read pulse generated by the reset circuit display timer is applied to the memory readout circuit. The read pulse transfers the decade counting unit final-count states to the memory readout circuit. The memory readout circuit causes a display of the accumulated N-Count on the glow-tube readouts. These displays are representative of the decimal N-Count in the associated decade counter unit circuits. Each totalized N-Count set into the readout display is held until the next read pulse changes the input flip-flop states of the memory readout circuit.

(5) If the parity circuits determine that a consistency error exists, the parity circuits will cause the memory readout circuit to display the preset number or all zeros.

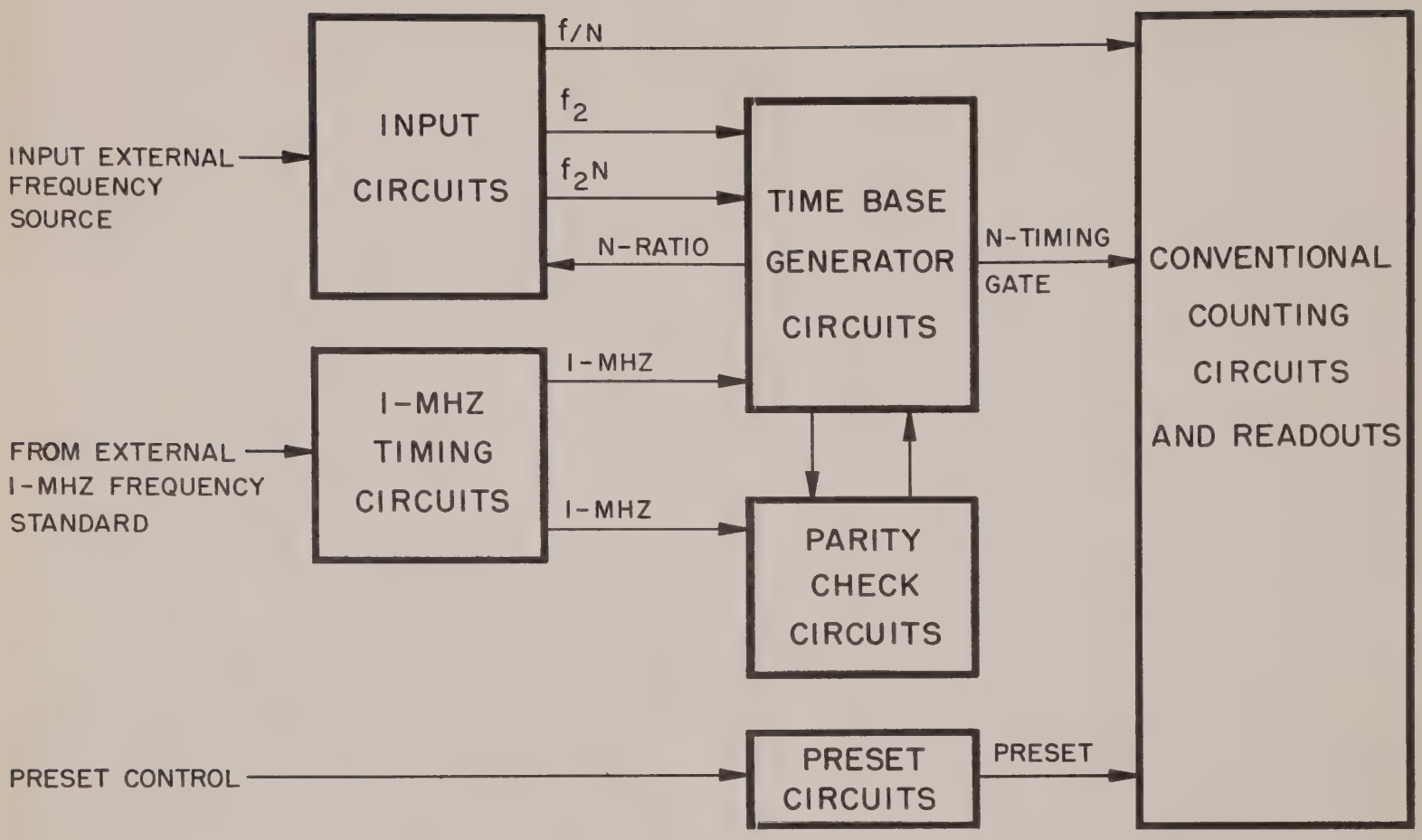

FIGURE 10. FREQUENCY COUNTER, SIMPLIFIED BLOCK DIAGRAM

23. DETAILED BLOCK DIAGRAM

a. The basic counter circuit functions are arranged to provide two modes of operation. These modes correspond to the three positions of the frequency range switch. The direct mode (low band) and the mid-high mode (mid and high bands). The sampling technique is used only in the mid-high mode of operation. Each arrangement includes a main gate with, (1) a signal input, and (2) an input control or gating signal. Following the main gate is a series of cascade decade counting units which accumulate and display the total number of pulses that are passed during the enabling of the gating signal. (See Figure 13.) The modes of operation are discussed in paragraph 24.

b. Circuit operation in the two modes is similar. Pulses are passed through the main gate to the decade counters for a predetermined period. The pulses are counted and the resultant measured frequency is displayed by the readout indicators. The primary difference is the method used to maintain a consistent accuracy check of the input frequency. In the direct mode the input sampling circuits (sampling technique) and the parity circuits are bypassed. In the mid-high mode of operation the range switch programs the instrument related to the particular band setting, as well as positioning the decimal light such that the frequency readout is always in megahertz.

24. OPERATING MODES

a. Direct Mode. In the direct mode of operation, the instrument functions as a conventional frequency counter, the range switch positioned in the low band controls the input signal distribution. The decade counting units of the counting unit count the total of input N-count pulses while the timing gate is held open. The count in the decade counting unit is then transferred to the readout circuit for display. The unknown frequency source is applied to the input jack and the signal is routed directly to the C.U. circuit of the counting unit. In the seven digit instruments the time base period in this mode of operation is fixed at 100 milliseconds. In the nine digit instruments the resolution switch sets the time base period.

b. Mid-High Modes. In either the mid or high mode of operation (see Figure 13) the frequency counter circuit arrangement permits control of the N-Timing gate by the time base generator circuit. The N-Time gate is opened for a controlled time interval (N-Timing period) and the accumulated count in the counting unit represents the number of input cycles or pulses passed. The controlled intervals (width of the N-Timing gate) will vary for the frequency being measured (from something more than 8 millisecond to something less than 90 milliseconds) on seven digit instruments. The intervals are automatically determined by the time base generator circuit.

25. DIRECT MODE FREQUENCY MEASUREMENT CYCLE.

The direct mode frequency measurement cycle (see Figure 11) is initiated as the reset pulse clears (or sets) all circuits to specific states. The end of the reset pulse generates the preset pulse. The range switch being in the low band position inhibits the input circuits and the parity consistency check functions. The input signal is coupled directly to the C.U. circuit in the counter chain. The range switch programs the I.S. and C.U. circuits such that the f input from the input divider is directed through a low pass filter in the I.S. circuit to the C.U. circuit through a switching relay.

a. N-Timing Gate Generation. The direct mode of operation N-timing gate is generated by the five decade dividers (in the time base) counting down the 1-MHz oscillator output. The reference oscillator output is squared in a shaper circuit located in the R and C circuit (A36). The clock output of the shaper is coupled through the time base delay (A37) circuit to drive the time base generator. In the direct mode no delay is acted on the clock signal and it is coupled uninhibited through this circuit. The clock is then counted down by the first three dividers A42, A43 and A44 in the time base generator chain. The overflow output of A44 is OR gated through the R and C circuit and drives the last two dividers A45 and A46. As the time base chain counts, each DCU produces a '9's signal. When a 9's carry coincidence occurs (e.g. all five DCU's at nine) a 9's carry pulse is ANDed from the time base generator. This resultant carry pulse is applied to the start-stop circuitry in the R and C circuit. To shorten the total time between reset and the start signal for a measurement cycle, the last three DCU's (A44, A45 and A46) are reset to a 9's condition. Thus the time between reset and start is reduced from 100 milliseconds to 100 microseconds. The N-Timing gate is the period between the first 9's carry output (start) to the next 9's carry output (stop). This gate will require the full count of the five cascaded DCU's. Therefore the N-Timing gate (for seven digit instruments) in the direct mode will have a fixed time duration of 100 milliseconds.

b. Start-Stop Flip-Flop Output. The negative-reset pulse resets the states of the start and stop flip-flop circuits to a predetermined condition. This action enables the circuits to react to the nine-carry pulses generated by the decade dividers. (The nine-carry pulses are constantly being generated but will not trigger the start-stop flip-flops until their gates are enabled.) Simultaneously with the resetting of the start-stop flip-flops, the first two dividers are reset to zero while last three dividers are reset to a nines count. This count serves to speed-up (or advance) the carry coincidence of the dividers outputs to the start flip-flop. Since the five dividers will be coincident every 100 milliseconds, the advancing of the coincident condition decreases the time interval after application of the reset pulse to 100 microseconds before the first carry pulse. The first carry pulse to occur after reset, sets the start flip-flop, resulting in the opening of the N-Timing gate. Due to the 1-MHz frequency and the number of dividers, the resultant time interval between the first carry pulse and the arrival of a second carry pulse will be 100 milliseconds long. The setting of the start flip-flop also enables the stop flip-flop gate and inhibits the start flip-flop gate. The arrival of the second carry pulse (100 milliseconds later) sets the stop flip-flop. The resultant action closes the N-Timing gate.

c. C.U. Circuit Gating. The N-Timing gate generated by the start-stop flip-flops is applied to the C.U. circuit as a gating pulse (N-Timing gate). The input frequency is applied to the C.U. circuit input and is counted by the counting chain during the interval the N-Timing gate enables the C.U. circuit input. If the input count exceeds the capacity of the count chain the overflow signal from the most significant digit (A19) triggers the overflow circuit (A21). This will turn on the number 1 overflow lamp. The number 1 overflow lamp goes out and the number 2 lamp turns on if two such overflows occur. Three overflows (which could occur only if the instrument was reset to a number other than zero) will turn on both lamps.

d. Totalized Count Display. The totalized count in the counter circuit is transferred to the memory readout circuits as a result of the display pulse generated by the stop flip-flop. The display pulse sets the read one-shot multivibrator which generates the read pulse. The read pulse then provides the transfer function to the memory readout circuit.

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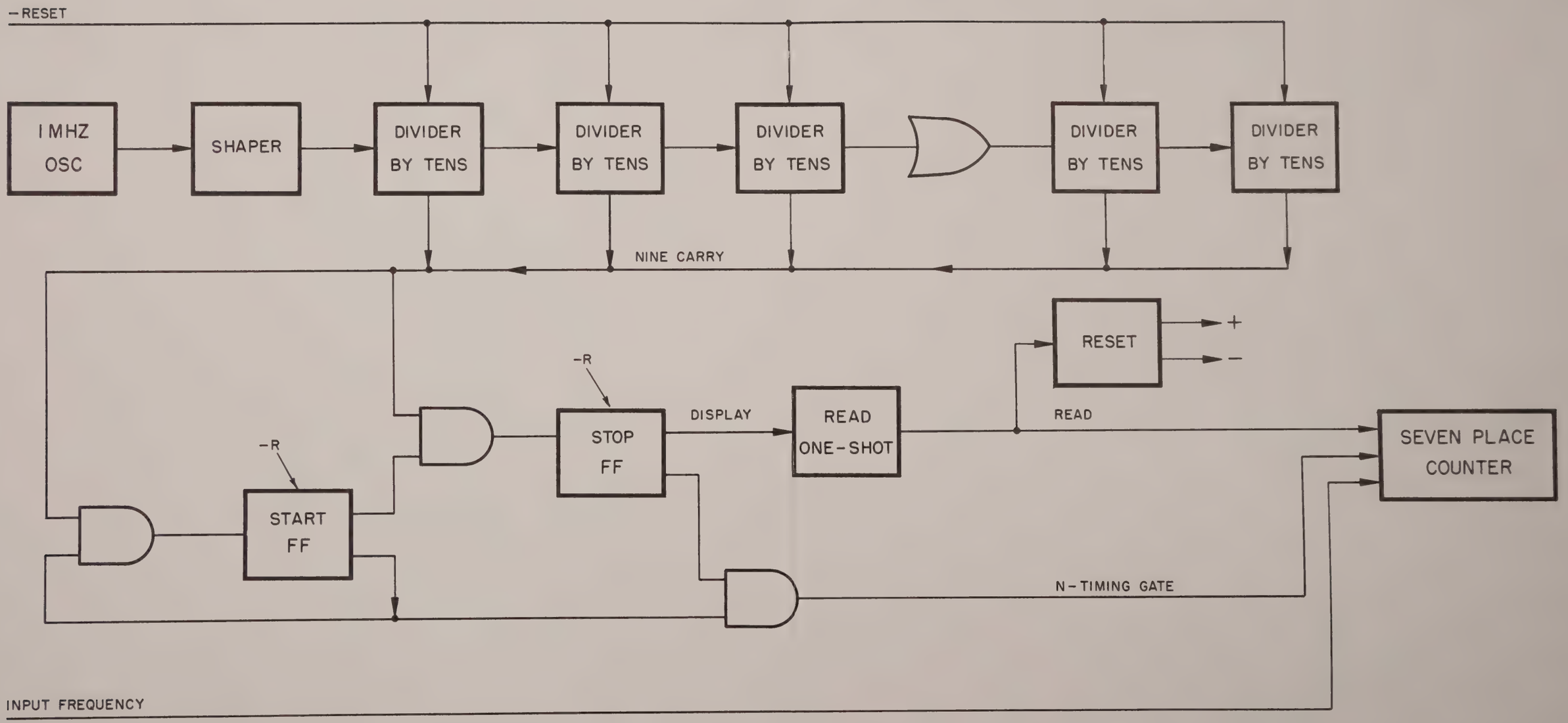


FIGURE 11. LOW BAND OF OPERATION, BLOCK DIAGRAM

e. Reset. Upon completion of a measurement cycle it is necessary to generate a reset signal. Setting the stop flip-flop initiates the chain of events which ultimately produces the reset pulse.

26. MID-HIGH MODE FREQUENCY MEASUREMENT CYCLE

The mid and high mode of frequency operation are similar except certain circuits are programmed by the range switch to function in a specific manner (see figure 13). The mid mode of operation extends from 90 megahertz to 850 megahertz and the high mode from 750 megahertz to 4 gigahertz on the Models 945/946, and to 6 gigahertz on the Models 950/951. The external frequency input (f) is processed by the input sampler circuits which provides the signal drive for the counting chain and the remaining signal processing circuits. *

a. Input Sampler. The input sampler consists of the power divider, the I.C. circuit, the F.S. circuit, and the I. S. circuit. The external frequency f is combined with the N-Ratio level from the R generator and gate centering circuit, and is processed as follows:

(1) The range switch programs the I.C. circuit (A3) and a resultant signal ratio is produced. This signal is processed by the S.C. circuit producing two outputs, one from coax connector A4-2 and the other from coax connector A4-3. The signal at terminal 2 will be a continuous signal between 9 and 10 megahertz or between 70 and 80 megahertz relative to the range switch being in the mid or high position respectively. The signal at terminal 4 will be a continuous signal 9 to 10 megahertz regardless of the range switch setting. Both signal outputs are identified on the block diagram as the ratio f/N. The input drive to the C.U. circuit and counting chain is taken from terminal 2 with the signal at terminal 3 driving the F.S. Circuit.

(2) The F.S. circuit (A1) combines the f/N output of the S.C. circuit with an internally generated 1.5 kilohertz signal f_2, and drives the I.S. circuit. This signal is identified as $f/N+f_2$. A second signal is developed in the F.S. circuit and is used as drive to the reset and A logic circuits. This signal is the 1.5 KHz sync (A24-17) which also is referred to as the short time base.

(3) The I.S. circuit is programmed by the range switch, In the mid-band (range) position the inputs f and $f/N+f_2$ are combined to produce the signal f_2N. In the high range position additional filtering is added allowing operation at the higher frequencies. The output is still identified as f_2N. F_2N is a continuous signal to the ratio gate circuit for further processing with the ratio gate signal from the A logic circuits.

b. Ratio Gate. The continuous f_2N signal (from the I.S. circuit) is applied to the ratio gate circuit (A29-16) for processing by the ratio gate pulse. The f_2 signal generated in the F.S. circuit and applied to the A logic circuit (A25-6) is divided by eight or two (in either the mid or high modes respectively), and the resultant output pulse is applied to the ratio gate circuit (A29-13). The f_2 signal is chopped by the ratio gate pulse to develop 4N pulses which are applied to the B logic circuit (A27-6). Each burst of 4N pulses applied to the B logic circuit is divided by eight or four (in the high or mid modes respectively) and the resultant bursts of Ns are applied to the parity logic (A26-2) for processing.

*The signals described are essentially for Mid Band operation. See Paragraph 26K for High Band signals.

c. Parity Consistency. These single-bursts-of-N are processed in the parity circuit to produce a one-burst-of-N output (A26-16). This is accomplished by the gating of the ratio gate flip-flop in the parity logic circuit. Since the ratio gate pulse applied to the ratio gate circuit (A29) is a function of the 1.5 KHz f_2 signal, an additional flip-flop (alternate reset) in the A logic circuit divides the f_2 signal once more. The resultant alternate reset pulse generated is applied to the ratio gate flip-flop in the parity logic circuit (A26-14). The alternate reset is exactly twice the time duration of the ratio gate. During the first half of the alternate reset, one burst-of-N is gated through to the ratio and control circuit (A36-13) for the development of the time base interval (N-Timing gate). The (-) negative swing of the alternate reset pulse clamps the gate closed, not to open again until a new counting cycle starts, beginning with (-R) reset. The second half of the alternate reset occurs as a second burst-of-N is gated through the "B" logic. This burst does not go to the ratio and control circuit, but combines with the first burst-of-N to determine whether they are odd or even. (If N is always odd or is always even, the result of the addition of the two will always be even). This addition takes place in the odd-even flip-flop in the "B" logic circuit Only if one signal is odd (7, 15, 19, etc.) and the other is even (8, 12, 16, etc.) will there be an odd condition existing in the odd-even flip-flop. The odd condition will then be presented to a two input AND gate, the other input coming from the parity enable circuit. Parity enable occurs for 30 microseconds and at the same time of the (+) positive swing of the alternate reset. If the two pulses are coincident, (the odd-even flip-flop set in an odd condition), an output pulse will be generated by the error reset one-shot and then applied to the reset circuit (A35-8) to interrupt the measurement cycle. If no consistency errors exist there will be no error reset.

d. Measurement Ratio. The two decade dividers in the ratio counter (A38 and A39) divide the pulses in the one burst-of-N pulses. The resultant division is used to develop the ratio of the burst-of-N and the N-Timing gate generated, and also reset the readout flip-flop in the ratio and control circuit (A36-10). The 1-MHz pulses bei ng divided by the time base decade dividers (A42 through A46 would normally automatically initiate the start-stop flip-flop circuits at a predetermined time after reset (see Paragraph 25 b). To assure that a time base width (N-Timing gate) will be long enough and also the ratio to the frequency being measured is correct, the readout flip-flop is set at the start of the N-Timing gate (enabled by the start flip-flop) to enable the readout gate that permits a certain number of 1-MHz pulses to be applied to the time base dividers A45 and A46. The number of pulses passed is determined by the one-burst-of-N signal that is processed by the ratio counter (A38, A39). The same number of 1-MHz pulses is applied to the ratio counter as is applied to the time base dividers, both being determined by the number of N pulses. The resultant action is to advance or speed-up the ultimate count in the ratio counter and the time base decade dividers.

e. Counting and Display. The resultant generation of the N-Timing gate pulse is then applied to the C.U circuit as described in Paragraph 25 c. The readout display is accomplished as described in Paragraph 25 d.

f. Reset. A reset pulse is generated upon completion of the measurement cycle. This is initiated by the display pulse taken from the stop flip-flop.

g. AD and R Generator Circuits. The AD and R generator circuits (found only in those instruments with Option A - Automatic Trigger Level) are used to produce an N-Ratio voltage level which in conjunction with the input circuits ultimately produce the N count input to the decade counting unit.

(1) The N-Ratio level is developed by the AD circuit, the divide-by-16, the divide-by-eight, and the ramp generator (R Generator) circuits. Circuit operation is such that the output N-Ratio level will seek a new value after three error resets are provided.

(2) The combined BCD outputs of the divide-by-16 and divide-by-eight circuits bias the R generator. The R generator output is the N-Ratio level.

(3) The AD circuit is triggered by error resets. If three or more error resets occur an output pulse is applied to the divide-by-16, divide-by-eight chain. This will change the bias level of the ramp generator and cause the N-Ratio level to step to a new value. A centering circuit acts upon the N-Ratio level to position it at the optimum operating point.

h. Time Base Delay Circuits. To permit a complete parity check and synchronize the clock input to the time base circuits, a control has been placed between the 1-MHz clock signal and the time base input. In the seven digit instruments the time period between the reset pulse and the start pulse (first nines coincidence) normally exceeds the time required to make a parity check and establish a go no-go condition. In nine digit instruments the resolution switch can reduce the time between the reset and start pulses such that the time base will begin making a frequency measurement before the parity circuits have been able to arrive at a decision. Therefore before the clock is applied to the time base the time base delay flip-flop must be set. This is accomplished by ANDing a trigger pulse to the flip-flop after the parity check has been completed. Setting the time base delay in this manner assures a frequency measurement will not be started prematurely. Two additional circuit functions are produced by the time base delay circuitry. They are the greater-than-90 detecting circuits which will produce an error reset if the ratio counter indicates a greater-than-90 count; and the remote preset generator circuitry which when programmed will preset the decade counting unit to a predetermined number.

i. Range Switch. The range switch performs the multiple function of programming various circuits within the instrument, positioning the decimal point indicator light, and print out. The decimal point is programmed to cause the frequency readout to be in MHz for all positions of the range switch. The range switch is a three position, two pole, rotary switch with four wafers. All wafers are the non-shorting type. A detailed drawing of the range switch is found on the range switch schematic D-3-4131. Detailed Block Diagram (Figure 13) of the seven digit instruments shows the various applications of the range switch with the particular wafer called out as to its function. The following is a breakdown of the range switch and its function. Wafer number one contains wipers A and B with six contacts. A1, A2, and A3 for wiper WA and B1, B2 and B3 for wiper WB. Wafer number two contains wipers C and D with six contacts. C1, C2 and C3 for wiper WC and D1, D2 and D3 for wiper WD. Wafer number three contains wipers E and F with six contacts. E1, E2 and E3 for wiper WE and F1, F2 and F3 for wiper WF. Wafer number four contains wipers G and H with six contacts. G1, G2 and G3 for wiper WG and H1, H2 and H3 for wiper WH.

(1) Low Band Position.

(a) Wiper WA and WG are connected to the +12 volt supply. Wiper WB is grounded. In the low band position contact A1 is connected to the C.U. circuit (A5-2). This programs the C.U. circuit such that the input frequency

(f) is applied from the direct input of the I.S. circuit (A31). ContactB1 is open and wiper B is not used in the low band position.

(b) Wiper WF is grounded. Contact F1 is connected to the decimal light (I1). In the low band position the frequency displayed will readout xx.xxxx MHz.

(c) Contacts B1, C1, D1 and G1 are not used.

(2) Mid Band Position.

(a) Wiper WA connects the +12 volt supply to contact A2 which programs the I.C. circuit (A3) enabling the 9 to 10 MHz astable multivibrator.

(b) Wiper WB grounds B2 which programs the A logic circuit (A25-7) to function in a divide-by-eight mode.

(c) Wiper WC is not used.

(d) Wiper WD grounds D2 which programs the S.C. circuit (A4) such that the divide-by-eight circuitry is inhibited.

(e) Wiper WE is connected to the error reset one-shot output of the P logic (A26-4). Contact E2 connects the error reset pulse to the AD circuit (A34-17) and the reset circuit (A35-8).

(f) Wiper WF grounds contact F2 which turns on the decimal light (I2) causing the frequency display to readout xxxx. xxx MHz.

(g) Wiper WG is connected to the +12 volt supply through WA Contact G2 is open and not used.

(h) Wiper WH grounds the Test/Normal switch through contact H2 placing the switch in the system.

(3) High Band Position.

(a) Wiper WA applies +12 volts to the I.C. circuit (A3-11) through contact A3. This programs the 70 to 80 MHz astable multivibrator.

(b) Wiper WB grounds contact B3 programming the A logic circuit (A25-10) to function in a divide-by-two mode.

(c) Wiper WC grounds contact C3 programming the gate and centering circuit (A29-15).

(d) Wiper WD grounds contact D3. D3 is an open connection and not used.

(e) Wiper WE performs the same function it did in the mid band, connecting the error reset pulse to the reset and AD circuits.

(f) Wiper WF performs the same function it did in the mid band, turning on the decimal light I2.

(g) Wiper WG applies +12 volts to contact G3 programming the I.S. circuit (A31-16). This causes the I.S. circuit to operate in a higher frequency range.

(h) Wiper WH grounds the test/normal switch through contact H3 as described in the Mid band position.

j. Resolution Switch. In the nine digit instruments (946/951) the resolution switch is added to complement the range switch. It provides four significant steps in programming the instrument; 1) it inserts the DCU's A40, A41, A42 and A43 into the time base chain, 2) it completes the nine's carry cycle for the DCU's as they are added, 3) it positions the decimal point indicator light on the readout display for a MHz frequency reading and the decimal point location at the print out jack, and 4) it produces a reset pulse each time it is positioned to a new setting. The resolution switch is a four position single pole rotary switch with nine wafers. All wafers except wafer number one are the non-shorting type. The following is a breakdown of the wafers. Wafer number one contains wiper WA and four contacts, 1A through 4A. Wafer number two contains wiper WB and six contacts, 1B through 6B. Wafer number three contains wiper WC and six contacts, 1C through 6C. Wafer number four contains wiper WD and six contacts, 1D through 6D. Wafer number five contains wiper WE and six contacts, 1E through 6E. Wafer number six contains wiper WF and six contacts, 1F through 6F. Wafer number seven contains wiper WG and six contacts, 1G through 6G. Wafer number eight contains wiper WH and six contacts, 1H through 6H. Wafer number nine contains wiper WJ and six contacts, 1J through 6J. Wafer number nine is used as a terminal board and wiper WJ is open.

(1) Range switch low band, resolution position I.

(a) Wafer number one wiper WA and contact 1A are not used in this position.

(b) Wiper WB of wafer two connects the time base delay circuit (A37-6) 1MHz clock signal through contact 1B to DCU A43-7 of the time base chain.

(c) Wiper WC of wafer three is connected to J12 terminal E for programming the 1 bit decimal point position on the print out jack. Contact 1C is returned to the -12 volt supply applying a "0" state to the #1 bit.

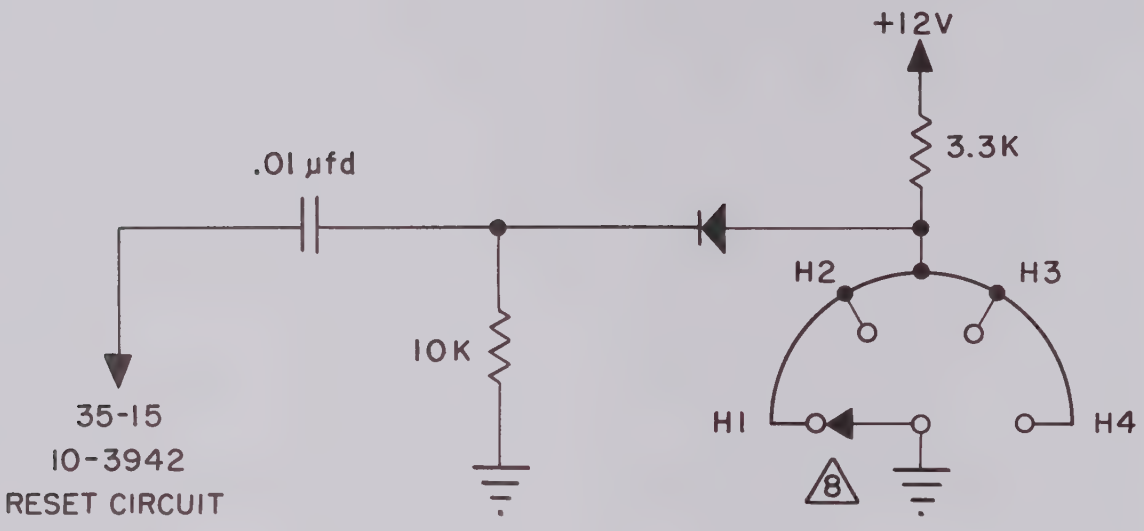
(d) Wiper WD of wafer four is connected to J14-14 for programming the #2 bit decimal point position on the print out jack. Contact 1D is connected to 1G and returned to the range switch terminal F2 and F3 through wiper WG. Contact 1D is also connected to the least significant digit (LSD) decimal light L1. Since this is an open circuit in this mode a "0" state is applied to the #2 bit and the light is off.

(e) Wiper WE of wafer five is connected to J12-14 for programming the #4 bit decimal point position on the print out jack. Contact 1E is connected to 1F and the decimal light L3. Wiper WF completes the circuit to terminal F1 on the range switch. Since the range switch is in the low band position this point is grounded by wiper WF of the range switch. This will cause the decimal indicator L3 to turn on and the frequency readout will be xxxxx.xxxx MHz. A "1" state is also applied to the #4 bit of the print out connector.

(f) Wafer six was described in (e) above.

(g) Wafer seven was descrived in (d) above.

(h) Wafer eight is wired as a simple pulse generator with wiper WH grounded and contacts 1H, 2H, 3H and 4H strapped together and returned to the +12 volt supply through a 3.3K resistor (See simplified drawing). The diode, the 10K resistor and the .01uf capacitor complete the circuit. As the switch is rotated, the momentary open between contacts causes a positive going pulse to be developed and coupled to the reset circuit through 35-15 producing a reset pulse.



(2) Range switch low band, resolution position II.

(a) Wafer one connects the nines carry line from A46-6 (the time base DCU) through wiper WA and contact 2A to the time base DCU A42, adding the nines carry function from A42.

(b) Wafer two connects the 1MHz clock to the time base DCU A42 adding another DCU to the chain.

(c) Wafer three-applies a "1" state to the #1 bit decimal point position on the print out jack.

(d) Wafer four remains an open circuit as described in (1) (d) above. A "0" state is reflected to the #2 bit through wiper WD contact 2D and decimal light L2.

(e) Wafer five applies a "1" state to the #4 bit of the decimal indicator on the print out connector through wafer six and the range switch.

(f) Wafer six causes decimal indicator light L4 to turn on by grounding contact 2F through wiper WF and the range switch. This will cause the frequency displayed to read xxxx.xxxxx MHz.

(g) Wafer seven is an open circuit in this position due to the range switch.

(h) Wafer eight will produce a reset pulse each time a new position is selected as described in (1) (h) above.

(3) Range switch low band, resolution position III.

(a) Wafer one connects the nines carry output of DCU A41 (in the time base chain) into the time base circuitry through wiper WA and contact 3A. A42's nines carry remains in the circuit due to the shorting characteristics of this wafer.

(b) Wafer two connects the 1MHz clock from A37-6 to A41-7 through wiper WB and contact 3B thus adding another DCU to the time base chain.

(c) Wafer three applies a "0" state to the #2 bit decimal point position on the print out jack through wiper WD, contact 3D, wafer six and the range switch.

(d) Wafer four applies a "1" state to the #2 bit decimal point position on the print out jack through wiper WD, contact 3D, wafer six and the range switch.

(e) Wafer five applies a "1" state to the #4 bit decimal point position on the print out jack through wiper WE and contact 3E.

(f) Wafer six turns on decimal light L5 by grounding contact 3F and wiper WF through the range switch. Thus the frequency readout becomes xxx.xxxxxxMhz.

(g) Wafer seven is an open circuit in this position.

(h) Wafer eight produces a reset pulse as previously described.

(4) Range switch low band, resolution position IV.

(a) Wafer one connects the nines carry output of DCU A40 to the time base chain through wiper WA and contact 4A. A41 and A42 remain in the circuit as previously described.

(b) Wafer two connects the 1MHz clock signal to DCU A40 through wiper WB and contact 4B added another DCU to the time base circuitry.

(c) Wafer three applies a "1" state to the #1 bit decimal point position on the print out jack through wiper WC and contact 4C.

(d) Wafer four applies a "1" state to the #2 bit decimal point position on the print out jack through wiper WD contact 4D wafer six and the range switch.

(e) Wafer five applies a "1" state to the #4 bit decimal point position on the print out jack through wiper WE and contact 4E.

(f) Wafer six turns on decimal light L6 by grounding contact 4F through wiper WF and the range switch causing the frequency readout to appear as xx.xxxxxxx MHz.

(g) Wafer seven is an open circuit in this position.

(h) Wafer eight produces the reset pulse as previously described.

(5) Rotating the range switch to the Mid and High position will be described only as to the positioning of the decimal point on the frequency display. When the range switch is positioned in the mid or high band setting control of the decimal lights shifts from wafer six to wafer seven. Wiper WF of wafer six is now open circuited, whereas wiper WG of wafer seven is grounded through the range switch.

(a) Resolution position I will cause the frequency display to read xxxxxxx.xx MHz through contact 1G, Wiper WG and the range switch turning on L1.

(b) Resolution position II will cause the frequency display to read xxxxxx.xxx MHz through contact 2G, wiper WG and the range switch turning on L2.

(c) Resolution position III will cause the frequency display to read xxxxx.xxxx MHz through contact 4G, wiper WG and the range switch turning on L3.

(d) Resolution position IV will cause the frequency display to read xxxx.xxxxx MHz through contact 4G, wiper WG and the range switch turning on L4.

k. Outputs of the Input circuits are influenced by the range switch. The following describes the two signal conditions in reference to the Mid or High Band setting of the range switch.

(1) The output at J2 of the IC circuit is f/N. N is determined by the range switch and will be a different value for the Mid and High Band setting.

(2) The f/N signal is processed by the S.C. circuit producing two outputs. In the Mid Band position the signal at J2 and J3 is f/N. In the High Band position the output becomes f/8N.

(3) The J2 output of the S.C. circuit, f/N or f/8N is further processed by the F.S. circuit producing a signal at J2 of $f/N + f_2$ or $f/8N + f_2$ for the Mid and High Band positions respectively.

(4) The J2 output of the F.S. circuit is further processed by the I.S. circuit producing at pin 6 the signals f_2N for the Mid Band or $8f_2N$ in the High Band setting of the range switch.

(5) Further processing takes place in the Ratio Gate and Ramp Centering Circuit. By action of the Ratio Gate signal from the A Logic circuit, the output at pin 17 of the Ratio Gate Circuit becomes 4N in the Mid Band and 8N if the High Band setting.

(6) Final processing takes place in the B Logic Circuit producing the N Ratio Signal at pin 11 by dividing the input by 4 in the Mid Band setting or by 8 in the High Band to produce N.

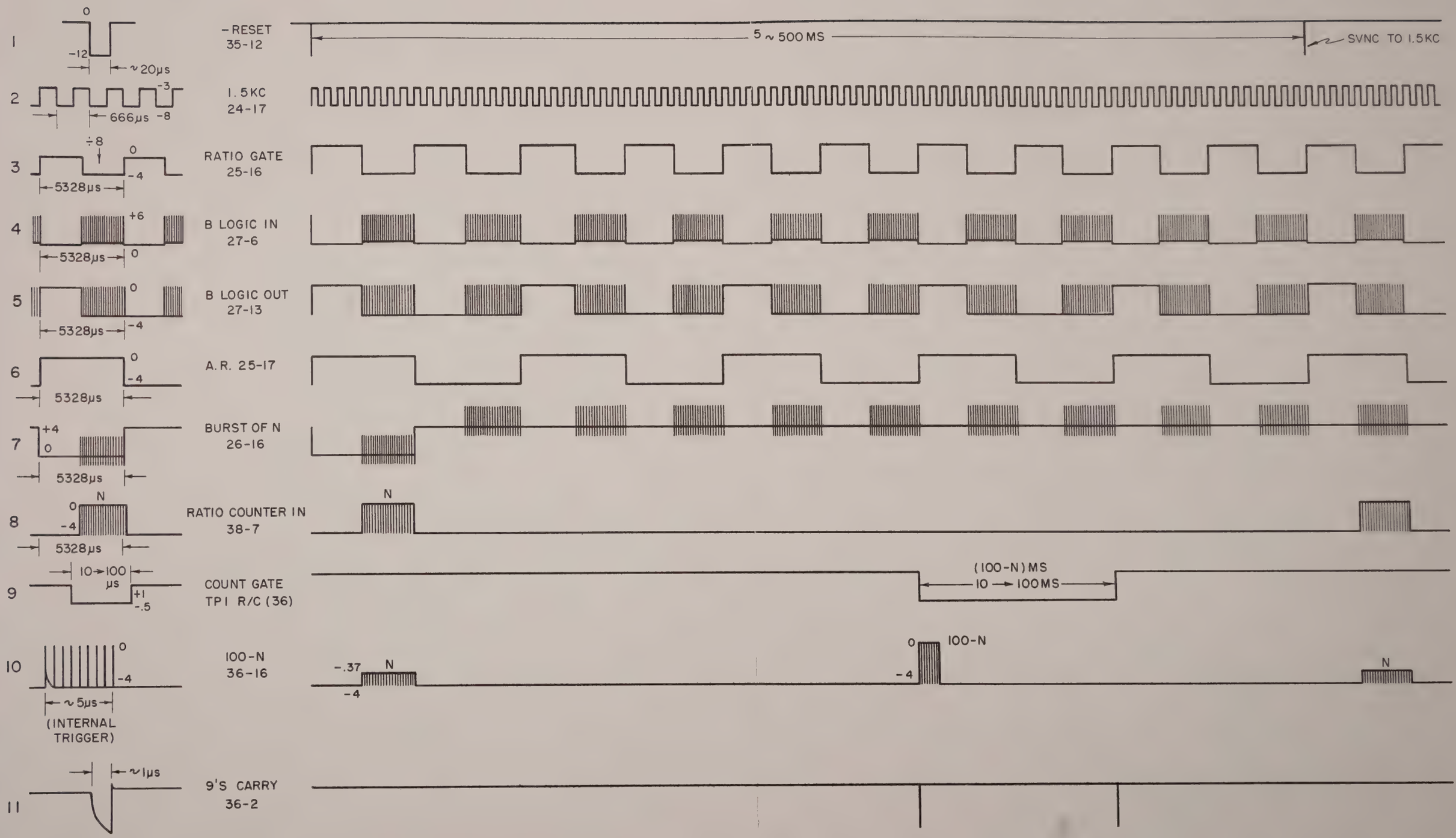


FIGURE 12. TIME BASE GENERATOR TIMING FUNCTIONS

LOGIC SYMBOL IDENTIFICATION

IN A B C → OUT: X = A·B·C — AND GATE

IN A B C → OUT: X = A+B+C — OR GATE

IN → OUT: AMPLIFIER

IN → OUT: GENERAL

Numerical Indicator

Decimal Light

① Overflow and Preset Light

SIGNAL FLOW

IN R T S → OUT 0 1

R = Reset — 0 = 0 Logic Level Out

T = Trigger — 1 = 1 Logic Level Out

S = Set

FLIP-FLOP

I C CIRCUIT = Printed Circuit Board Name

10-3994 = Assembly Part Number

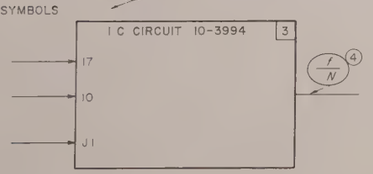
[3] = Chassis Location

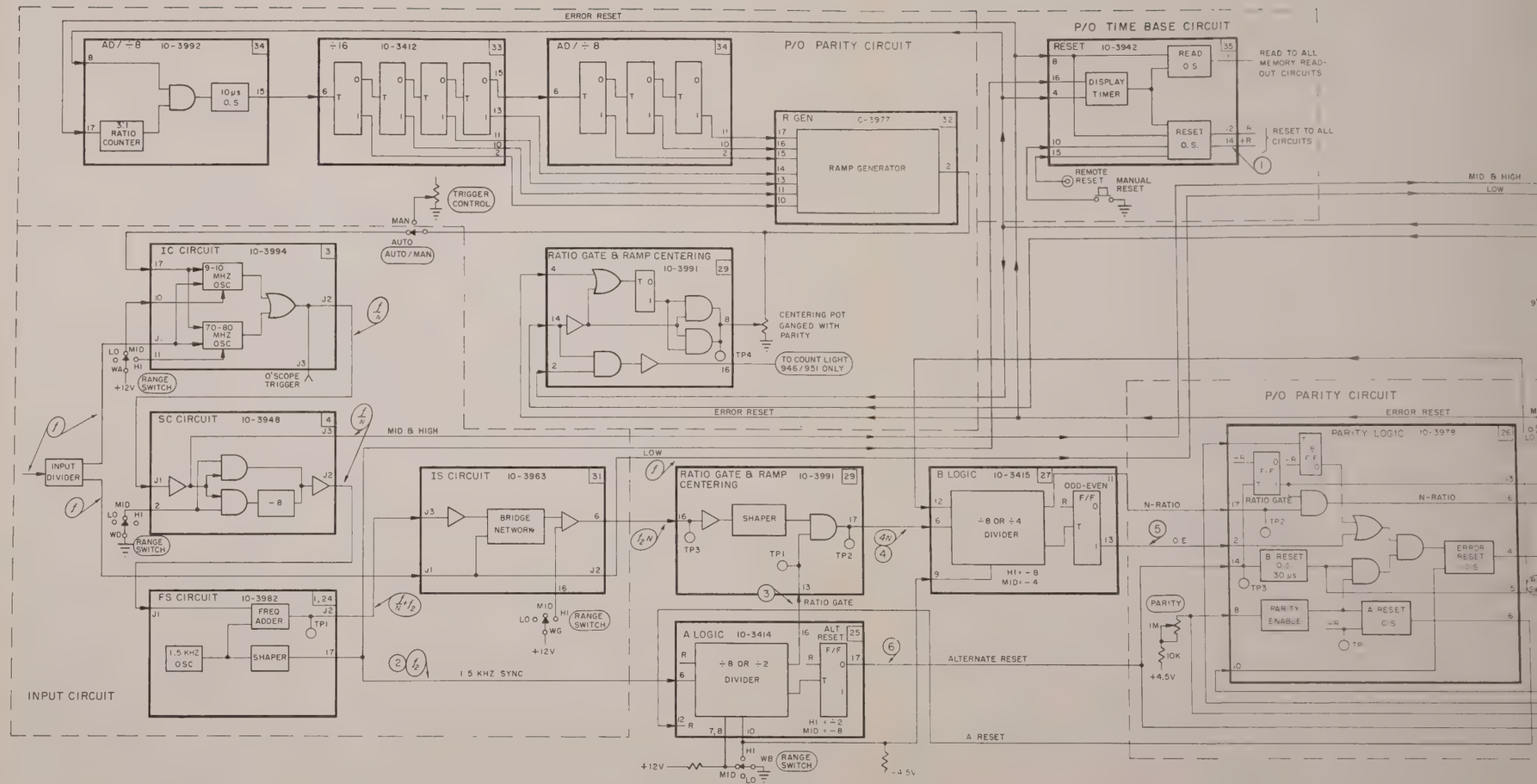
J1 or 17 = Input and Output Terminals or Connectors

(4) = Waveform Number on Figure 12

$\frac{f}{N}$ = Waveform Identification (All waveforms are labeled for Mid-band position of Range Switch.)

CIRCUIT BOARD SYMBOLS





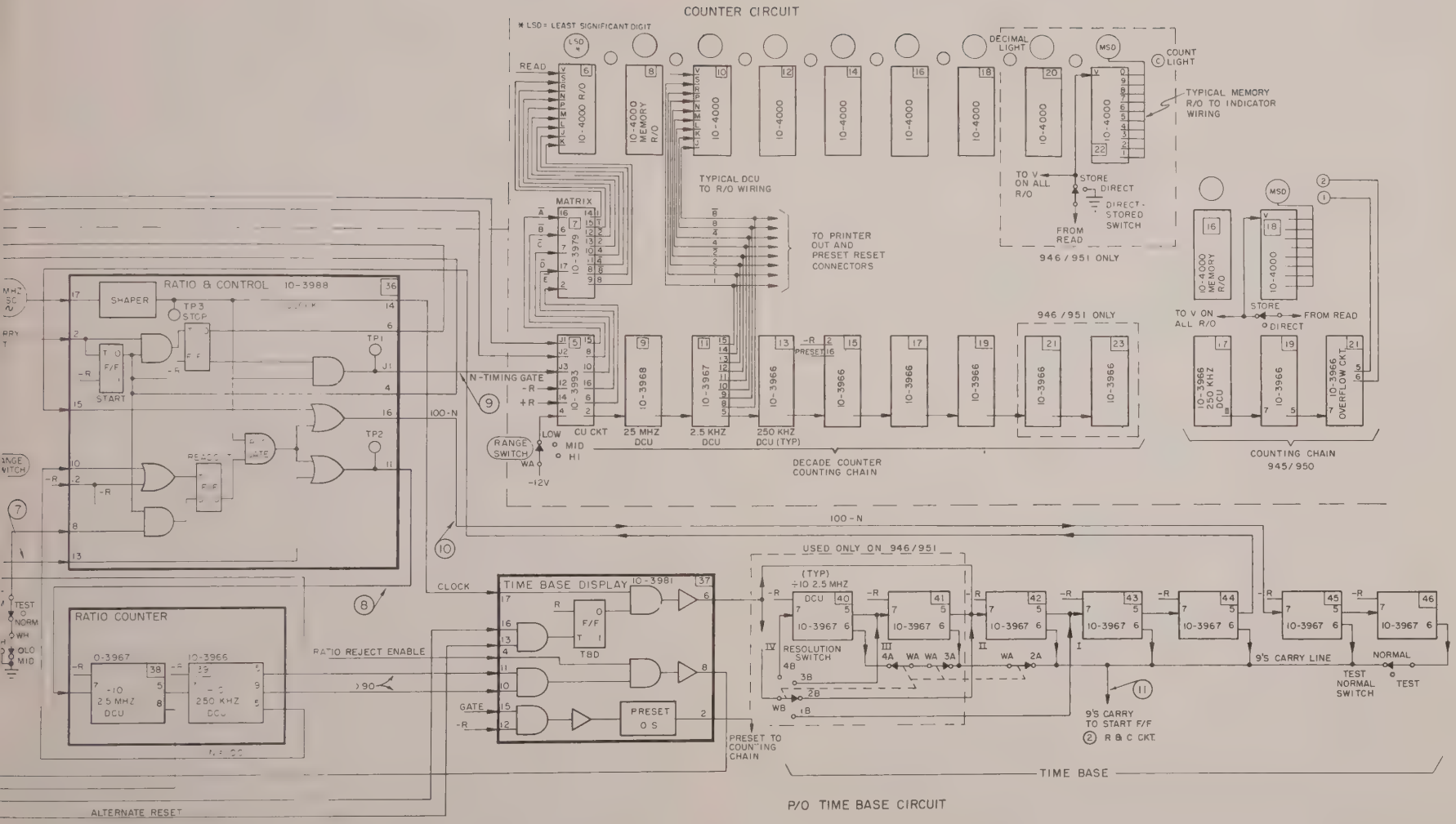


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FIGURE 13. FREQUENCY COUNTER 900 SERIES
DETAILED BLOCK DIAGRAM
85/86

27. GENERAL

This section provides the theory of operation of the individual printed circuit boards (except the input circuits), the dc power supply assembly and the associated controlling circuits. The input circuits (A1, A3, A4, A5, A29 and A31 - see Figure 13) circuits design are proprietary and only limited coverage is included, such as; types of output signals obtained and where, calibration and adjustments of controls.

28. CIRCUIT DESCRIPTION

The frequency counter circuit functions are discussed in the following paragraphs. Signal paths and waveforms are shown in the block diagram or on related timing diagrams. For complete circuit details, refer to the printed circuit board schematic diagrams in Chapter 7.

a. I.C. Circuit, (A3). The I.C. circuit processes the f input frequency with the N-Ratio level voltage supplied from the ramp generator circuits to develop the f/N frequency that is applied to the S.C. circuit.

b. S.C. Circuit, (A4). The S.C. circuit further processes the f/N signal supplied by the I.C. circuit and develops the f/N (N-Count) signal that is applied to the C.U. circuit and the counting circuits. The f/N signal is also applied to the F.S. circuit.

c. F.S. Circuit, (A1). The F.S. circuit generates the f_2 slow time base 1.5 KHz signal used by the reset and A logic circuits. The f/N signal supplied from the S.C. circuit is further processed and applied as the $f/N + f_2$ signal to the I.S. circuit for further processing.

d. I.S. Circuit, (A31). The I.S. circuit develops the f_2N signal from the $f/N + f_2$ signal supplied by the F.S. circuit and the f input frequency supplied from the power divider assembly.

e. Ratio Gate Circuits, (A29). The ratio gate circuits processes the f_2N signal supplied from the I.S. circuit with the ratio gate pulse supplied from the A logic circuit to develop continuous bursts of 4N signal. The 4N signal is applied to the B logic circuit for further processing.

f. C.U. Circuit, (A5). The C.U. circuit processes the f/N signal (supplied from the S.C. circuit) while the N-Timing gate (Supplied from the ratio and control circuit) is enabled. The C.U. circuit divides the N-Count by ten and drives the remaining decade counting circuits. The C.U. output is also used by the matrix circuit (A7) and becomes the least significant digit in the display.

g. 25-MHz Decade Counting Unit Circuit, (A9). The 25-MHz decade counting unit circuit is a high-speed binary-coded decimal counter that counts (and divides by ten) the one-tenth N-Count output from the C.U. circuit. A block diagram of the 25-MHz decade counting unit is shown in Figure 14. (Circuit timing is also shown in Figure 14). The decade divider is an arrangement of four cascaded binaries (flip-flops) that generates an output pulse for every ten input pulses. Consequently, when a frequency is applied to the counter input, the first binary divides it by two (since the first pulse switches the binary to the opposite state and a second pulse is required to return it to its original state). The output from the first binary is applied to the second binary through an emitter follower and an AND gate. The AND gate is enabled by the state of the fourth binary. The first binary output is again divided by two in the second binary (making a total division by four) and so on, with an expected total division of sixteen at the output of the fourth binary. By gating, the output from the second and third binary is applied to the fourth binary. Due to this gating action

(bypassing some otherwise required inputs) the expected division by sixteen is reduced to a division by ten.

The AND gate isolates the third binary output from the fourth binary input after the fourth binary is set. After the tenth pulse is received, the desired final output pulse is produced by a gating-ahead pulse applied to the fourth binary (D stage) by the first binary. The setting of the fourth binary inhibits the AND gate between the first and second binaries, and enables the nine-carry AND gate. The ninth pulse is applied to the nine-carry AND gate and an output is produced. Since the AND gate between the first and second binaries is inhibited, the tenth pulse output from the first binary is fed-ahead to the fourth binary (D stage) to reset it. The fourth binary resets to produce the tenth pulse which also results in all the binaries returning to zero. A carry pulse is thus transferred through amplifier Q9 which act as the input trigger to the next stage. Resetting the 25-MHz decade counting unit to zero is similar to the resetting to zero function discussed for decade counters in Paragraph 19 o (4). Electrical readout is obtained in a similar manner as discussed for decade counters in Paragraph 19 o (6). Refer to memory readout circuit, Paragraph k for decimal display function details.

h. 25 MHz Decade Counting Unit Circuit, (A11, A38, A42, A43, A44, A45 & A46). The 25 MHz decade counting unit circuit serves as a decade counter in the counting circuit or in the time base generator circuit. Operation is similar to that described for the 25 MHz decade counting unit discussed in Paragraph 28 g. A noted exception is the removal of Q10 the emitter follower stage. There is no display array connected to the binaries when used in the time base generator circuit. A block diagram and timing functions of the decade counting unit is shown in Figure 15. A decade counting unit is an arrangement of four cascaded binaries (flip-flops) that generates one output pulse for every ten input pulses. Consequently, when a frequency is applied to the input, the first binary divides it by two (since the first pulse switches the binary to the opposite state and a second pulse is required to return it to its original state). The resultant output of the first binary is again divided by two in the second binary (making a total division by four). This process continues in each binary with an expected total division of sixteen at the output of the fourth binary. The desired division by ten is obtained by gating in front of the second binary. (After the ninth input pulse is received the binaries will be in a state corresponding to a count of nine pulses.) The ninth pulse will set the fourth binary, then the tenth pulse resets the fourth binary. The ninth and tenth pulses provide the desired final output pulse. When used in the time base generator, the nine-carry output pulse is applied to a common nine-carry line with the other decade counting units. When all the decade counting units (time base) contain a coincident nine-carry, an output pulse will occur from the decade counting unit circuit. The nine-carry pulse serves to trigger the start-stop flip-flop in the ratio and control circuit. On the tenth input a carry pulse is transferred through Q9 to the following stages. Resetting the decade counting unit to zero is similar to the resetting to zero function discussed for the decade counters in Paragraph 19 o (4). Electrical readout is obtained in a similar manner as discussed for the decade counters in Paragraph 19 o (6). Refer to memory readout circuit, Paragraph k for decimal display function detail.

i. 250 KHz Decade Counting Unit Circuit, (A13, A15, A17, A19, A39). The 250 KHz decade counting unit circuit serves as a decade counter in the counting circuit or in the time base generator circuit. Operation and timing is similar to that described for the 2.5 MHz decade counting unit discussed in Paragraph 28 g. A noted exception is the removal of emitter follower Q10 and carry amplifier Q9. There is no display array connected to the binaries when used in the time base generator circuit. A block

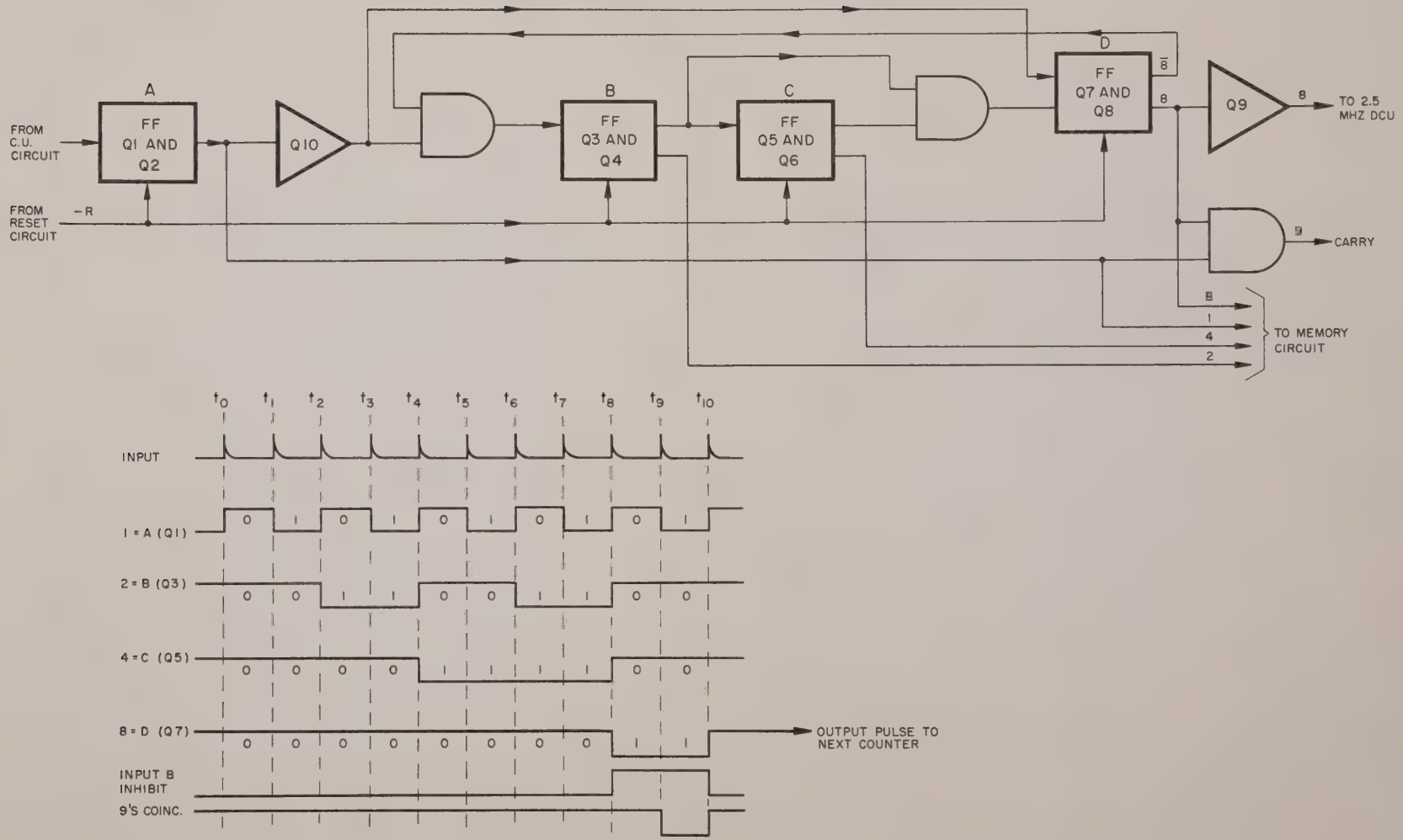
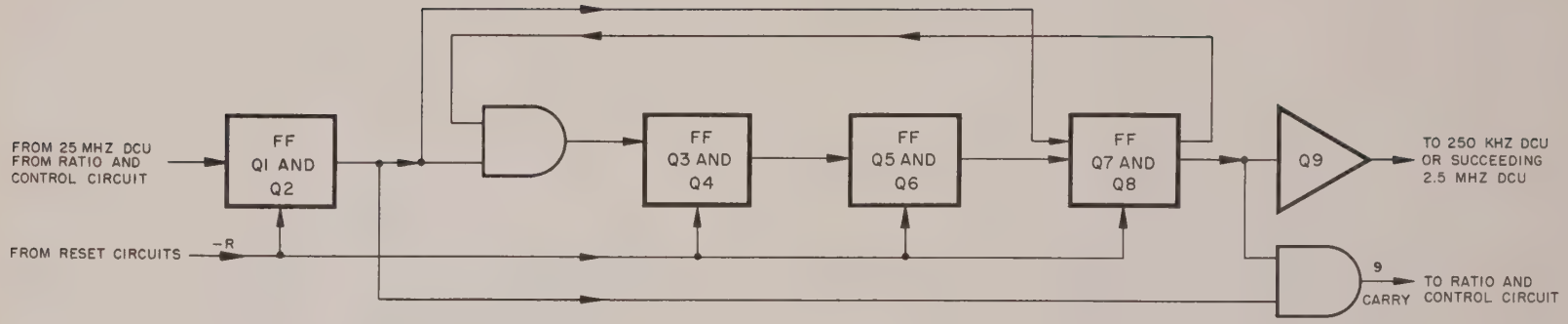


FIGURE 14. 25-MHZ DECADE COUNTING UNIT
BLOCK DIAGRAM



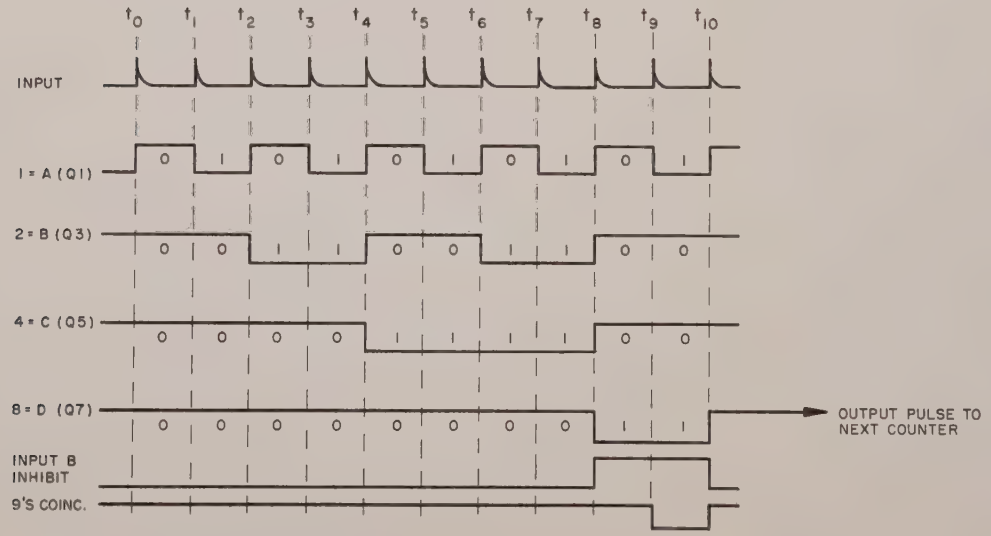


FIGURE 15. 2.5-MHZ DECADE COUNTING UNIT
BLOCK DIAGRAM

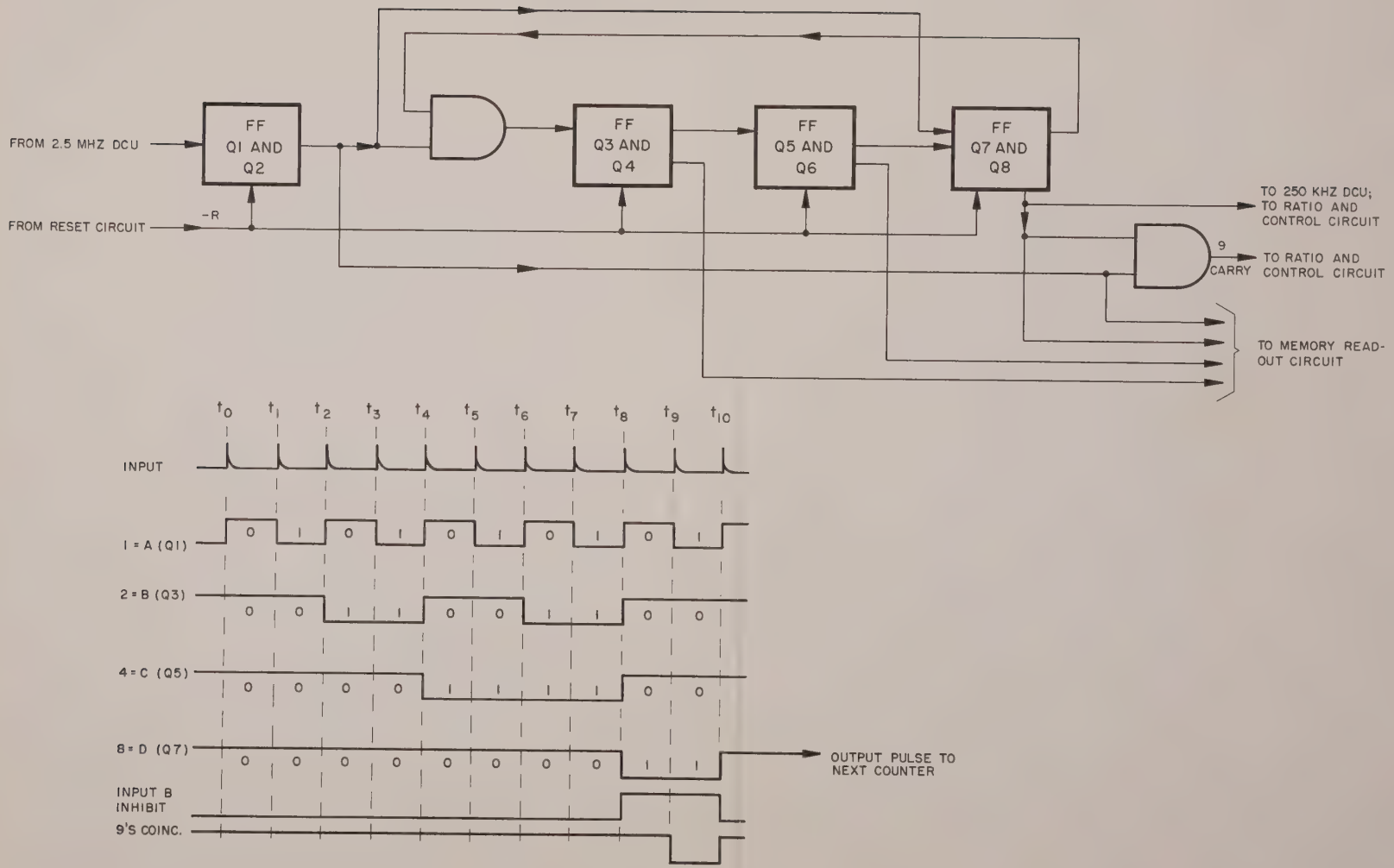

FROM 2.5 MHZ DCU
FF Q1 AND Q2
FF Q3 AND Q4
FF Q5 AND Q6
FF Q7 AND Q8
FROM RESET CIRCUIT
-R
TO 250 KHZ DCU; TO RATIO AND CONTROL CIRCUIT
9 CARRY
TO RATIO AND CONTROL CIRCUIT
TO MEMORY READ-OUT CIRCUIT
t0 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10
INPUT
1 = A (Q1)
2 = B (Q3)
4 = C (Q5)
8 = D (Q7)
OUTPUT PULSE TO NEXT COUNTER
INPUT B INHIBIT
9'S COINC.

FIGURE 16. 250-MHZ DECADE COUNTING UNIT BLOCK DIAGRAM

diagram and timing functions of the decade counting unit is shown in Figure 16. A decade counting unit is an arrangement of four cascaded binaries (flip-flops) that generates one output pulse for every ten input pulses. Consequently, when a frequency is applied to the input, the first binary divides it by two (since the first pulse switches the binary to the opposite state and a second pulse is required to return it to its original state). The resultant output of the first binary is again divided by two in the second binary (making a total division by four). This process continues in each binary with an expected total division of sixteen at the output of the fourth binary. The desired division by ten is obtained by gating in front of the second binary. After the eighth input pulse is received the binaries will be in a state corresponding to a count of eight pulses. When the ninth and tenth pulses are received the desired final output pulse is produced. When used in the time base generator the nine-carry output pulse is applied to a common nine-carry line with the other decade counting units. After all the decade counting units contain a coincident nine-carry, an output pulse will occur from the decade counting unit circuit. The nine-carry pulse serves to trigger the start-stop flip-flop in the ratio and control circuit. Resetting to zero is similar to the resetting to zero function discussed for the decade counting unit in Paragraph 19 o (4). Electrical readout is obtained in a similar manner as discussed for the decade counting unit in Paragraph 19 o (6). Refer to memory readout circuit, Paragraph k for decimal display function details.

j. Matrix Circuit (A7). The matrix circuit amplifies and decodes the output from the C.U. circuit. The decoded 8-4-2-1 binary output functions are then applied to the memory readout circuit flip-flops to be further decoded. A block diagram of the matrix circuit is shown in Figure 17 with circuit timing functions.

(1) Bi-Quinary Input. The C.U. circuit, which divides the input frequency being measured by 10 provides a quinary electrical readout of the accumulated count stored in its binaries. Since the memory readout circuits function with a binary 8 input, the quinary 5 output from the C.U. circuit requires further decoding (converting) to a usable type code.

(2) Matrix Operation - Amplifiers Q10 through Q17 amplify the matrix circuit quinary input levels and then apply them to the decoding matrix circuits to generate the binary 8 output. Five functions (A=0, $\overline{B}$=1, $\overline{C}$=0, $\overline{D}$=1, and $\overline{E}$=0) are supplied from the C.U. circuit. The matrix circuit is designed to cause the input levels to revert to a normal state if an input level is absent; that is, a flip-flop remains in the state to which it was set, while a differential amplifier will revert back to its original state when the input level is absent. The differential amplifier will revert back to its original state due to a constant bias level on one half of the amplifier circuit which will cause conduction in the associated transistor. Since the differential amplifier outputs from the matrix circuit are applied to flip-flops in the memory readout circuit, the reverting action back to an original state will also cause the generation of a reset pulse to the associated flip-flop.

k. Memory Readout Circuits, (A6, A8, A10, A12, A14, A16 and A18). The memory readout circuits serve to convert the binary weights developed in the decade counting unit or matrix circuit to a decimal value. This value is displayed on the numerical readout indicator in a decimal form. A block diagram of the memory readout circuit is shown in Figure 18. Each memory readout circuit contains four flip-flop circuits that are connected to binaries in an associated decade counting unit.

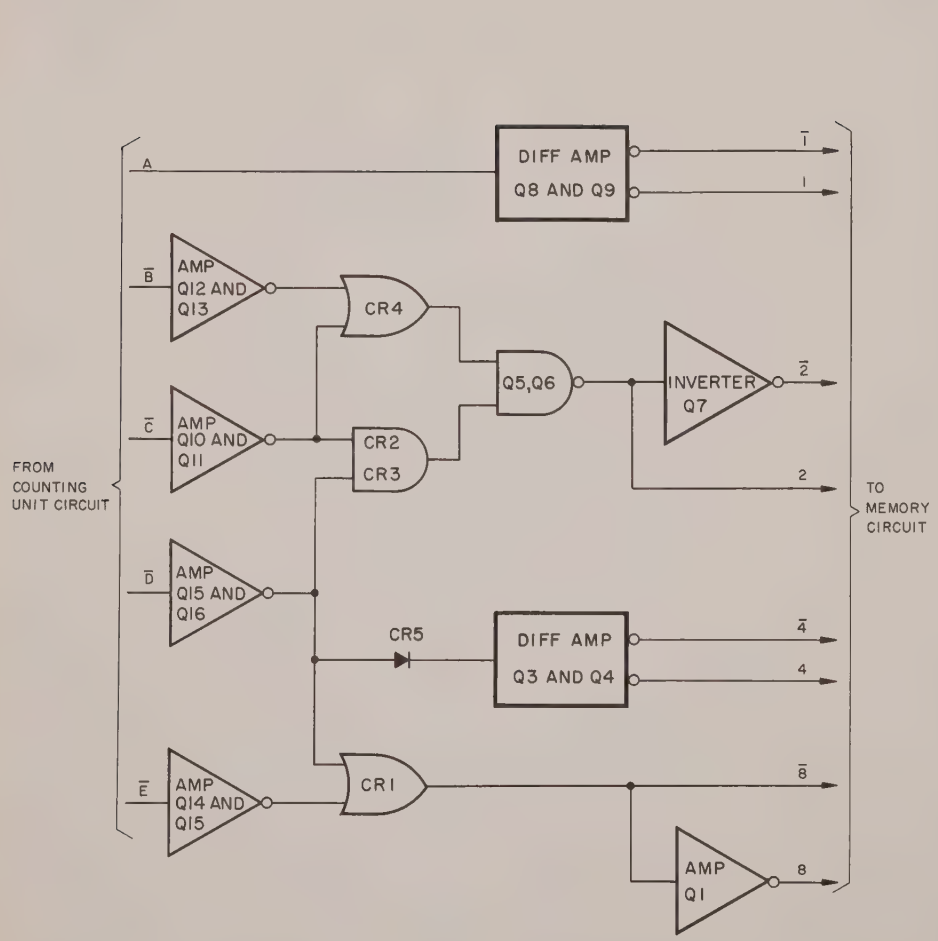
The four flip-flops are simultaneously set when the read pulse (supplied from the reset circuit) is applied to the individual memory readout circuits by the display pulse. The resultant state that is set into the four flip-flops is applied to resistor decoding gates. This sets the bias level to the numerical indicator tube driver transistor. The output from the resistor decoding gates is applied to additional decoding gates that drive the individual numerical elements in the readout tube.

(1) Read Amplifier. The read amplifier (Q19) is normally biased to remain cutoff. The resultant collector output bias voltage developed at the junction of R3 and R4 (see memory readout schematic) will be between +10 and zero volts depending on the conduction state of the circuit. The voltage level is used to inhibit the flip-flops in the memory readout circuit from changing states until the read pulse is applied to the memory readout circuit. This bias voltage is applied to the four flip-flop circuits through isolation resistors, R6, R11, R14, R19, R22, R27, R30 and R35.

(2) Flip-Flop Inhibiting. The bias voltage developed by the read amplifier, biases the bases of transistors Q1 through Q8 to a level above the emitter bias levels (between +2 to +5 volts). When the read amplifier conducts, the bias level drops to a negative level below zero volts. This bias level enables the input flip-flop to function normally; that is, change their states as determined by the weight of the signal applied to their individual bases.

(3) Flip-Flop Setting. The associated input decade counting unit flip-flop weights, supplied through isolating resistors, are applied to the bases of the flip-flop chain. One weight will be high (1) and the other will be low (0). The high level will be near zero volts and the low level will be near -9 volts. If the bias level applied to Q1 is high, (zero volts), Q1 will cutoff and Q2 will conduct. The resultant voltage levels developed at the collector of each transistor is applied to the emitters of alternate gates which drive the readout glow tube elements. These two lines determine the odd or even decimal number to be selected.

(4) Numerical Indication Selection. Assume the number 1 is to be illuminated. The BCD code required and applied to the flip-flops will be 0001. Flip-flops Q2, Q3, Q5 and Q7 are required to be in a conductive state. The collector output level at Q1 sets a low condition to the readout glow tube drivers Q10, 12, 14, 16 and 18. High input levels (1) are applied to decoding gate comprised of resistors R40, R45 and diode CR1. The gate is enabled and produces a high level output. The resistor gate output is applied to the bases of Q9 and Q10 which enables the driving transistors. Since Q1 (the odd line) enables the emitter of Q10, the voltage level causes Q10 to conduct ionizing the numeral indicator 1.



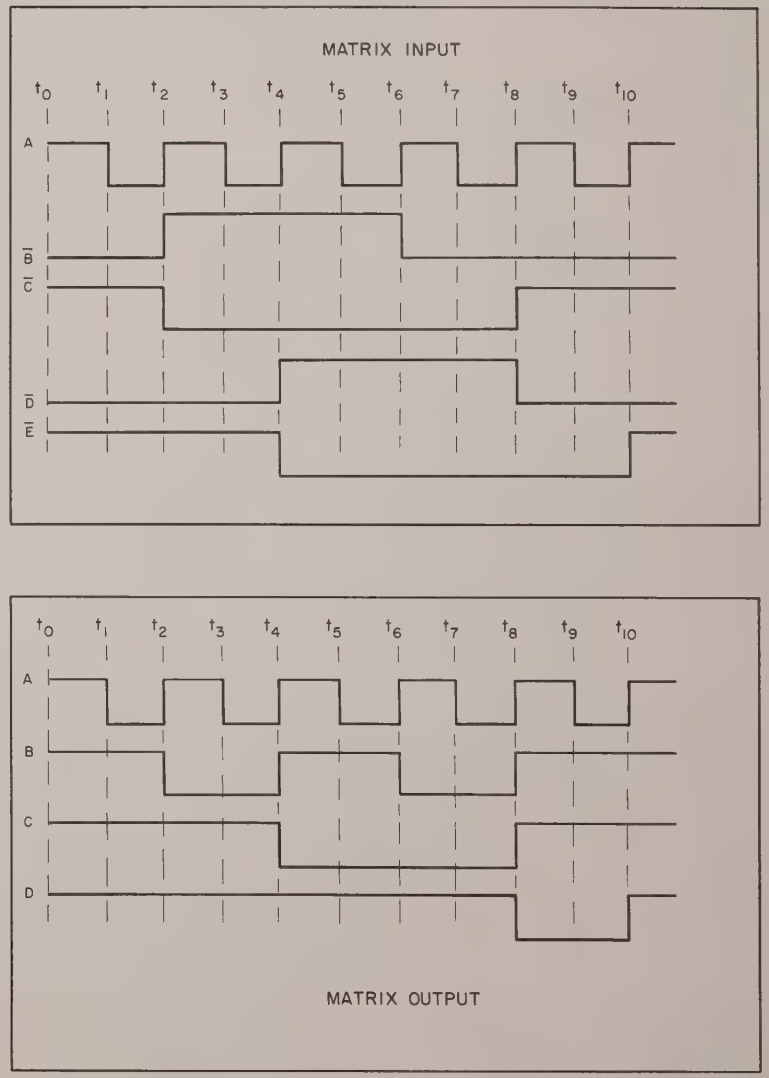


FIGURE 17. MATRIX CIRCUIT, TIMING FUNCTIONS AND BLOCK DIAGRAM

(5) Numerical Indication Selection Truth Table.

Decimal #	On State Decoding Binaries	On State Numerical Driver	Decoding R's	BCD Input Code 8421
1	Q2-Q3-Q5-Q7	Q10	R40, R45, CR1	0001
2	Q1-Q4-Q5-Q7	Q11	R38, R44	0010
3	Q2-Q4-Q5-Q7	Q12	R38, R44	0011
4	Q1-Q3-Q6-Q7	Q13	R41, R43	0100
5	Q2-Q3-Q6-Q7	Q14	R41, R43	0101
6	Q1-Q4-Q6-Q7	Q15	R39, R42	0110
7	Q2-Q4-Q6-Q7	Q16	R39, R42	0111
8	Q1-Q3-Q5-Q8	Q17	R46	1000
9	Q2-Q3-Q5-Q8	Q18	R46	1001
0/10	Q1-Q3-Q5-Q7	Q 9	R40,R45,CR1	0000

(6) Readout Indicator Tube. The readout indicator is a cold-cathode type glow-tube containing an inert gas. A positive 330-volts dc is applied through a current limiting resistor to the anode of the tube to excite the gas. When an element gate is enabled, the associated cathode which is connected to ground, causes ionization of the inert gas surrounding the element. The ionization will appear in the numerical shape of one of the ten digits.

(7) Readout Indicator Tube Illumination. Since the number one cathode is in series with Q10 the gas surrounding the number one elements becomes ionized. The element will remain ionized until the four flip-flops are reset (by the read pulse) to display another digit arrangement.

(8) Illumination of Remaining Numbers. The remaining numbers are individually illuminated in a similar manner. The voltage levels set by the flip-flops are applied to resistors R38 through R44 to develop enabling levels to the gates driving the remaining numbers. As the various levels are set by the flip-flops, and the read pulse, the individual gate to the element is enabled.

1. A.D. Circuit, (A34). The A.D. circuit is a trigger generator for the ramp generator input divider circuits. A block diagram of the A.D. circuit is shown in figure 19. The A.D. circuit will produce a trigger to change the N-Ratio level when the parity circuits cause an error reset. To inpart stability and minimize spurious triggering three such error resets are needed to trigger an output. Also the A.D. circuit is inhibited during display time. The A.D. circuit consist of a one-shot trigger generator Q9/Q10, gates CR11, 12 and 13 and amplifiers Q7 and Q8.

(1) Error reset pulses applied to Q8 charge integrating capacitor C15 through gate CR13. Diode CR14 clamps any positive transients that may be present to ground. Gate CR11 is held off by the cut-off state of Q7. Successive error resets will charge C15 until the one-shot Q9/Q10 is brought into conduction. Q9 conducting will partially

discharge C15. Each time the one-shot is triggered the N-Ratio level is stepped to a new value.

(2) During display time the negative going display pulse brings Q7 into conduction. Q7 conducting inhibits CR13 and integrating capacitor C15 is completely discharged.

m. Divide-By-16 Counting Unit Circuit, (A33). The divide-by-16 counting unit circuit serves as a simple frequency divider to provide voltage level inputs to the ramp generator circuit. A block diagram of the divide-by-16 counting unit is shown in Figure 19. The divide-by-16 counting unit circuit is an arrangement of four cascaded binaries (flip-flops) that generates one output pulse for every 16 input pulses from the A.D. circuit. The first binary divides the frequency by two (since the first pulse switches the binary to the opposite state and a second pulse is required to return it to its original state). The resultant first binary output is again divided by two in the second binary (making a total division by four). This process continues in each binary with an expected total division of sixteen at the output of the fourth binary. The sixteenth pulse is applied to the divide-by-8 counting unit for further division. The four binaries voltage level outputs (weights) are applied to the ramp generator circuit inputs for further processing.

n. Divide-By-8 Counting Unit Circuit, (A34). The divide-by-8 counting unit circuit serves as a simple frequency divider to provide voltage level inputs to the ramp generator circuit. A block diagram of the divide-by-8 counting unit is shown in Figure 19. Operation is similar to that described for the divide-by-16 counting unit discussed in Paragraph m. In this case the weights of the three binaries are also applied to the ramp generator circuit. The divide-by-8 counting unit circuit is an arrangement of three cascaded binaries (flip-flops) that generates one output pulse for every eight input pulses supplied from the divide-by-16 counting unit circuit. The first binary divides the input by two (since the first pulse switches the binary to the opposite state and a second pulse is required to return it to its original state). The resultant frequency is again divided by two in the second binary (making a total division by four). This process continues in each binary with an expected total division of eight at the output of the third binary. Therefore, after the eighth pulse is received, the binaries will have returned to the same state following the reset pulse. The three binary voltage level outputs are applied to the ramp generator circuit inputs for further processing. A total of 128 pulses are required to reset the combined binaries (divide-by-16 and divide-by-8 counting unit circuits) to their original states.

o. Ramp Generator Circuit (A32). The ramp generator serves to generate the N-Ratio level voltage applied to the I.C. circuit. A block diagram of the ramp generator circuit is shown in Figure 19. The ramp generator circuit contains seven differential amplifier circuits. The amplifiers are connected in such a manner as to cause the state of any of the seven differential amplifier output transistor to affect the final output voltage level from the ramp generator circuit. Each differential amplifier output-transistor-base is connected to the output-transistor-base in the other differential amplifiers. The associated collectors are connected to a common voltage divider summing network. The voltage divider is arranged to connect the collectors of the differential amplifiers in a series arrangement. The differential amplifier input transistor conduction state is determined by the weight of the related flip-flop input supplied from the divide-by-16 or the divide-by-8 counting units. The first differential amplifier (Q13 and Q14) output transistor collector voltage level (which will be high or low depending on whether the transistor is in a nonconduction or a conduction state), is weighed as a binary number and then algebraically summed with the output

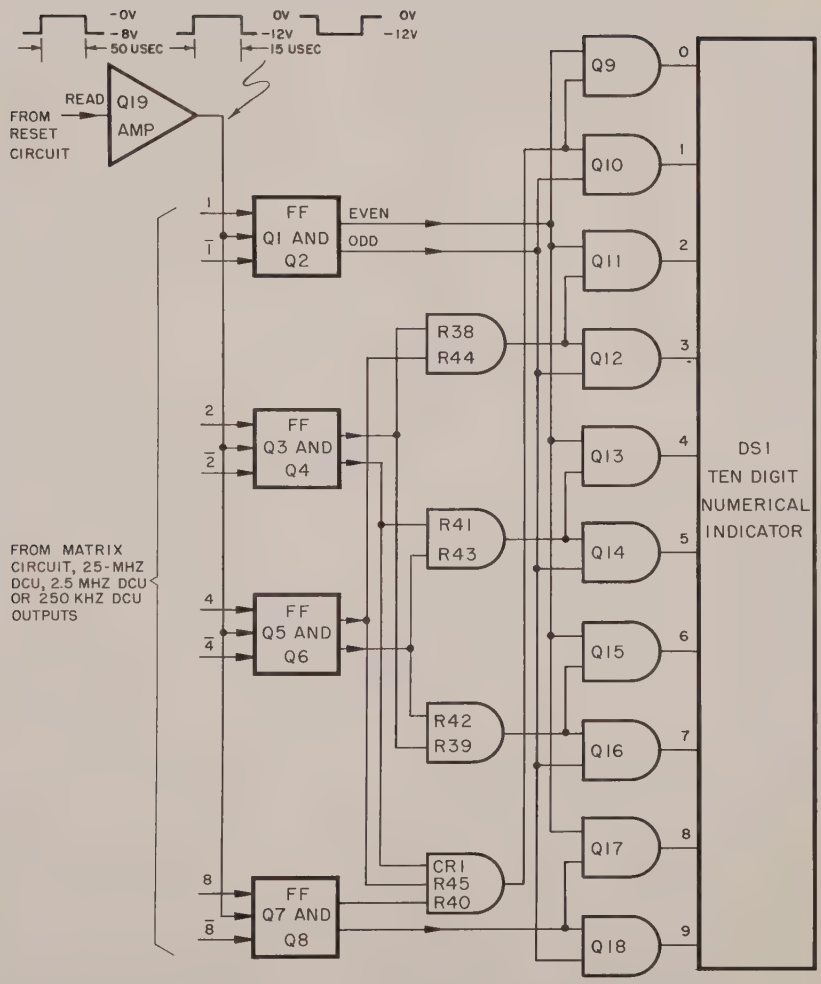


FIGURE 18. MEMORY READOUT, BLOCK DIAGRAM
101/102

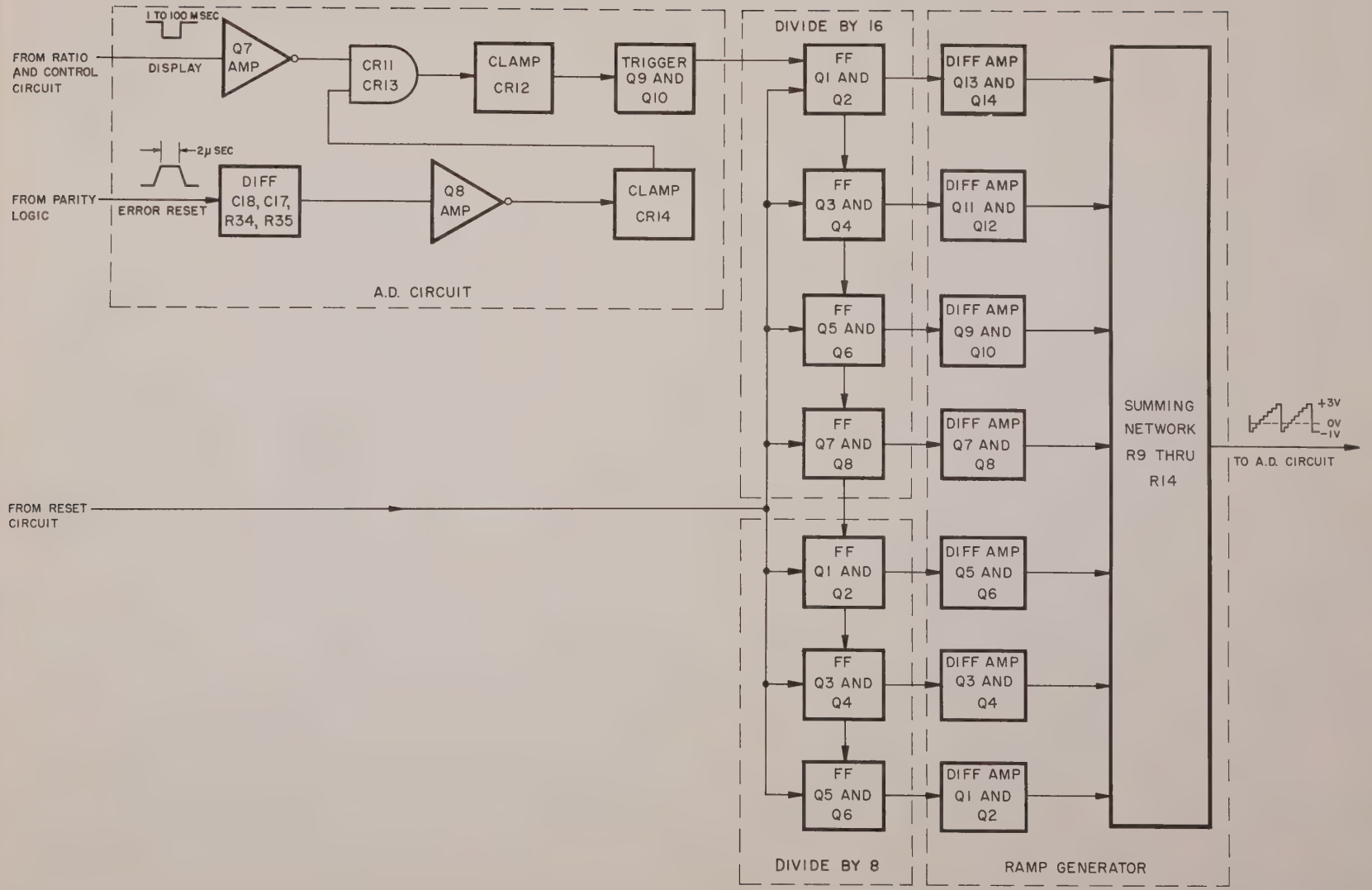


FIGURE 19. A.D. CIRCUIT, ÷16, ÷8 AND RAMP GENERATOR BLOCK DIAGRAM

from the second differential amplifier weight to develop a voltage level that will be between -1 and +3 volts. The states of succeeding differential amplifiers, properly weighed, are also summed. If the outputs from the differential amplifier transistors are in a conduction state, the transistor collector outputs will be at a low voltage level, and the resultant voltage output level from the ramp generator will be -1 ±0.3 volts. If the outputs from the differential amplifier transistors are in a non-conduction state, the transistor collector outputs will be at a high voltage level, and the resultant voltage output level will be +3 ±0.3 volts. The voltage level will remain at a final level as long as no additional input pulses from the A.D. circuit are applied to the divide-by-16 counting unit causing the counting units to change state. During normal operation, if the input frequency applied to the frequency counter changes, the N-Ratio value will also change (due to error reset pulses generated by the parity logic circuit) to maintain the S.C. circuit output between a nine to ten megahertz frequency. If a higher N-Ratio value is required, the parity logic circuit generates an error reset pulse which causes the ramp generator to change the N-Ratio level that is applied to the I.C. circuit. If this level and subsequent higher levels are unsatisfactory, that is, a lower N-Ratio level is required, the parity logic circuit detects this unsatisfactory condition and the ramp generator is caused to recycle through to the lowest level (0) and start generating a new N-Ratio level. The ramp generator circuit output may have several N-Ratio levels that will work for any given frequency. The ramp generator circuit output is applied to the I.C. circuit as the N-Ratio voltage level for further processing.

p. 'A' Logic Circuit, (A25). The A logic circuit serves to divide the f_2 sync frequency (supplied from the F.S. circuit) and to develop the ratio gate pulse applied to the ratio gate circuit. A block diagram of the A logic circuit is shown in Figure 20. Operation of the A logic circuit is similar to that described for the divide-by-16 counting unit, Paragraph m.

(1) The A logic circuit is an arrangement of four cascaded binaries (flip-flops) that generates two output pulses. When the 1.5 KHz sync (slow time base) frequency is applied to the input of the binary the first binary divides it by two (since the first pulse switches the binary to the opposite state and a second pulse is required to return it to its original state). The resultant output is again divided by two in the second binary (making a total division by four). This process continues in each binary with an actual total division of sixteen at the output of the fourth binary. The eighth pulse is received and the third binary generates an output pulse which is then applied to the ratio gate circuit as the ratio gate pulse. This pulse develops the burst of 4N signal from the f_2N frequency supplied from the I.S. circuit. The resetting of the third binary also serves to set the fourth binary which develops the alternate reset pulse. The alternate reset pulse is applied to the ratio gate flip-flop (A26Q8 and A26Q9) in the parity logic circuit.

(2) During operation the frequency range switch selects the proper mode of division. The switch applies disabling voltages to transistors A25Q4 and A25Q6 to prohibit a flip-flop action to occur in the circuits. The resultant action causes the second and third binaries to act as emitter followers, resulting in a division by two in the A logic instead of the division by eight.

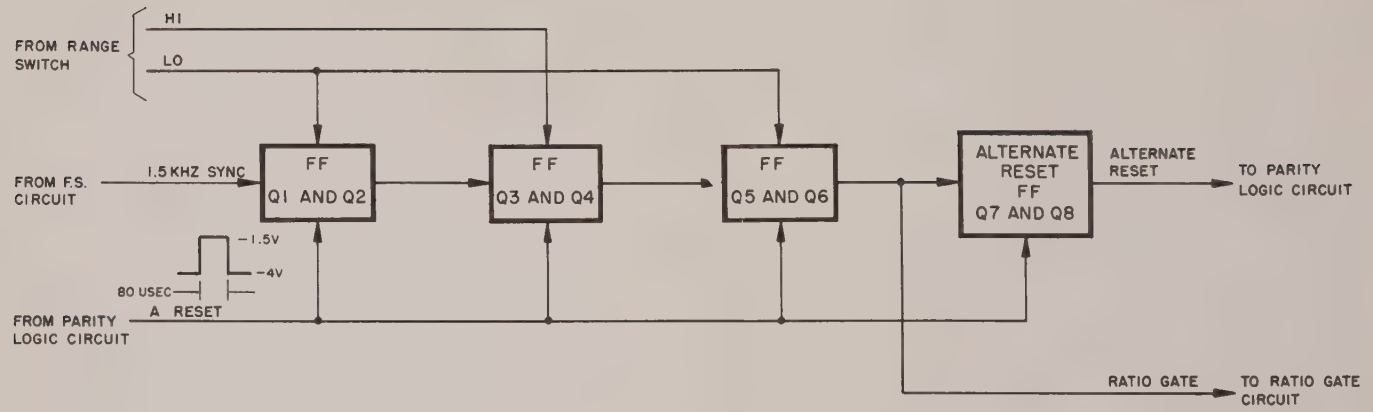
q. B Logic Circuit, (A27). The B logic circuit divides the burst-of-4N signal from the ratio gate circuit and develops a single-burst-of-N signal. The single-burst-of-N is then applied to the parity logic circuit for further processing.

A block diagram of the B logic circuit is shown in Figure 21. Operation of the circuit is similar to that described for the A logic circuit and discussed in Paragraph p. The action of the B logic circuit is to divide-by-four the 4N signal with a resultant single-burst-of-N frequency output generated. The B logic circuit is an arrangement of three cascaded binaries (flip-flops) that generates two output pulses. When the 4N signal is applied to the input, the first binary divides it by two. The resultant first binary output is divided again by two in the second binary (making a total division of four), and so on, with an expected total division of eight at the output of the third binary. After the third input pulse is received, the binaries will be in a state corresponding to a count of three pulses. The fourth pulse resets the first binary. The first binary output resets the second binary. The second binary output is then applied to the parity logic circuit as the single-burst-of-N signal. The third binary develops a check signal (odd-even pulse) which is used to develop the consistency check function in the parity logic circuit. The third binary counts the number of N present in the burst-of-4N signal. Two successive counts are made resulting in the third binary being reset to its normal state. If the third binary output states results in a set condition, the weight of the third binary is applied to the odd-even gate (A26Q3 and A26Q4) in the parity logic circuit as an odd condition. This alerts the computation error check circuit that an inconsistency exists, since the sum of the two identical bursts-of-N signal must be even. The B logic binaries are reset by the alternate reset pulse (from the A logic circuit) that is delayed 30 microseconds by the 30 microsecond delay gate (A26Q1 and A26Q2) in the parity logic circuit.

r. Parity Logic Circuit, (A26). The parity logic circuit provides the consistency check function of the counter frequency measurement. A block diagram of the parity logic circuit is shown in Figure 22. During normal operation, the burst-of-N signal is applied to the parity logic circuit for checking. If the frequency counter is computing accurately, the burst-of-N signal is allowed to pass through the parity logic circuit and is applied to the ratio and control circuits for further processing. If the parity logic circuit determines that a consistency error exists, an error reset pulse is generated that is applied to the reset circuit. The error reset pulse triggers the reset circuit, resetting the frequency counter circuits and initiating a new frequency measurement cycle.

(1) The burst-of-N signal, supplied from the B logic circuit, is applied to AND gate CR9. The ratio gate flip-flop (Q8 and Q9) is also connected to this AND gate. The flip-flop is intially set with Q9 cut off. The alternate reset pulse supplied from the A logic circuit is also applied to the ratio gate flip-flop. The alternate reset pulse does not set the ratio gate flip-flop until the alternate reset pulse goes to a reset state. Therefore, the first burst of N-signal will be passed through the AND gate and applied to the ratio and control circuit for further processing. When the Ratio Gate flip-flop is in a set state the burst-of-N is inhibited at the AND gate.

(2) After the burst-of-N signal is processed in the ratio and control circuit the signal is applied to the ratio counter (A38 and A39). The NOT (level) function from the fourth binary in the first decade counter (A38) is returned to the greater-than eight flip-flop (A26Q10 and A26Q11). The greater-than eight flip flop is initially set with Q10 cutoff. The burst-of-N signal is divided once more while still in the B logic circuit to develop the odd-even pulses. The odd-even pulse is applied to OR gate Q3 with the greater-than-eight pulse from the decade counter. If the generated odd-even pulse ends in an odd condition, or the greater-than-eight flip-flop output is less than eight, the OR gate generates an output pulse. This pulse is



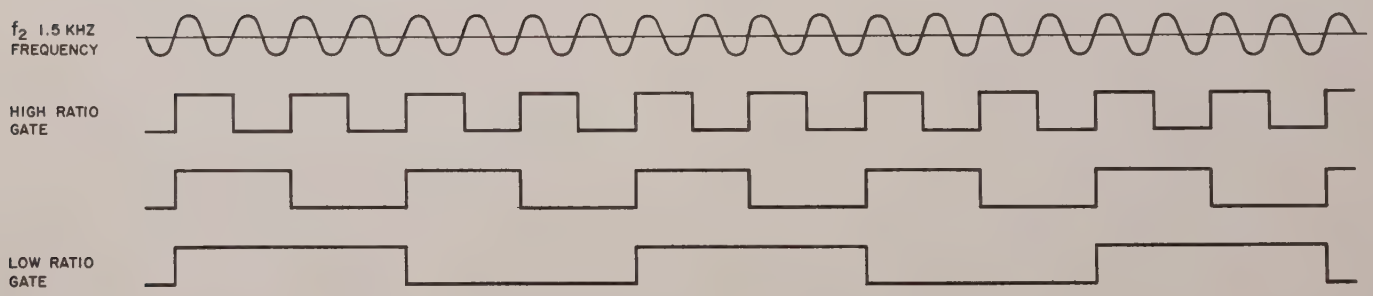


FIGURE 20. A LOGIC, BLOCK DIAGRAM AND TIMING FUNCTIONS

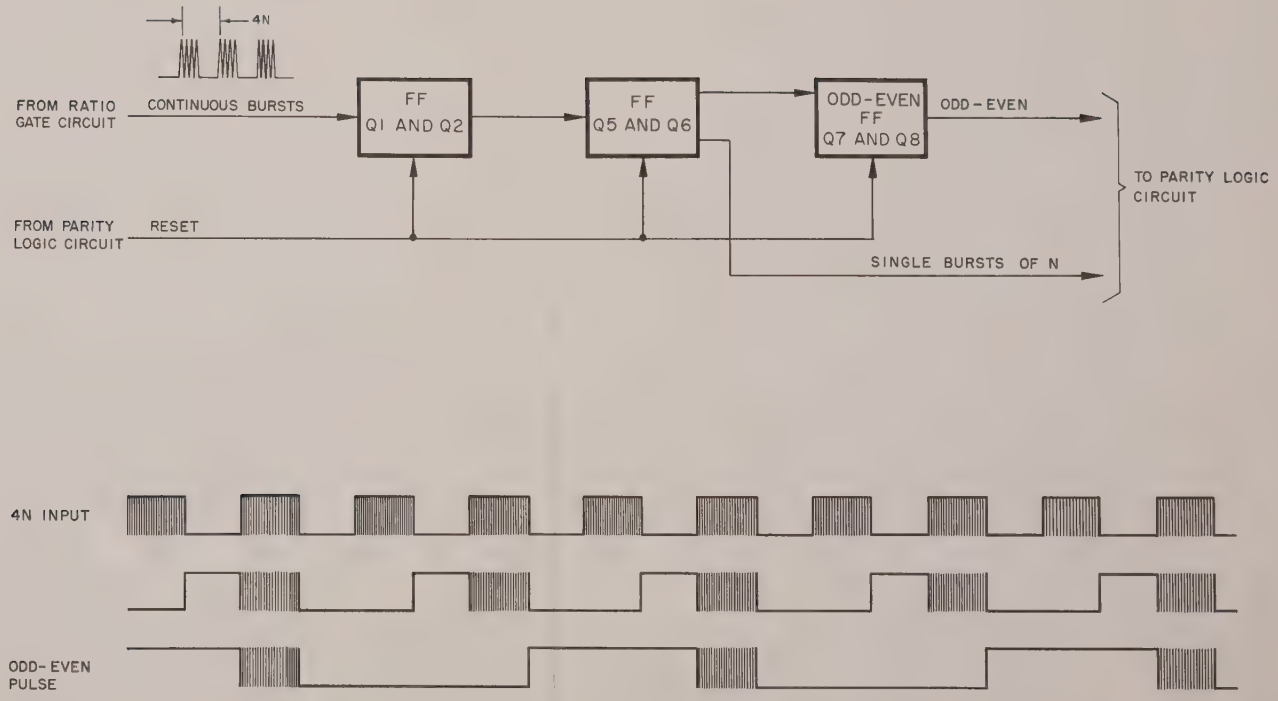


FIGURE 21. B LOGIC, BLOCK DIAGRAM AND TIMING FUNCTIONS

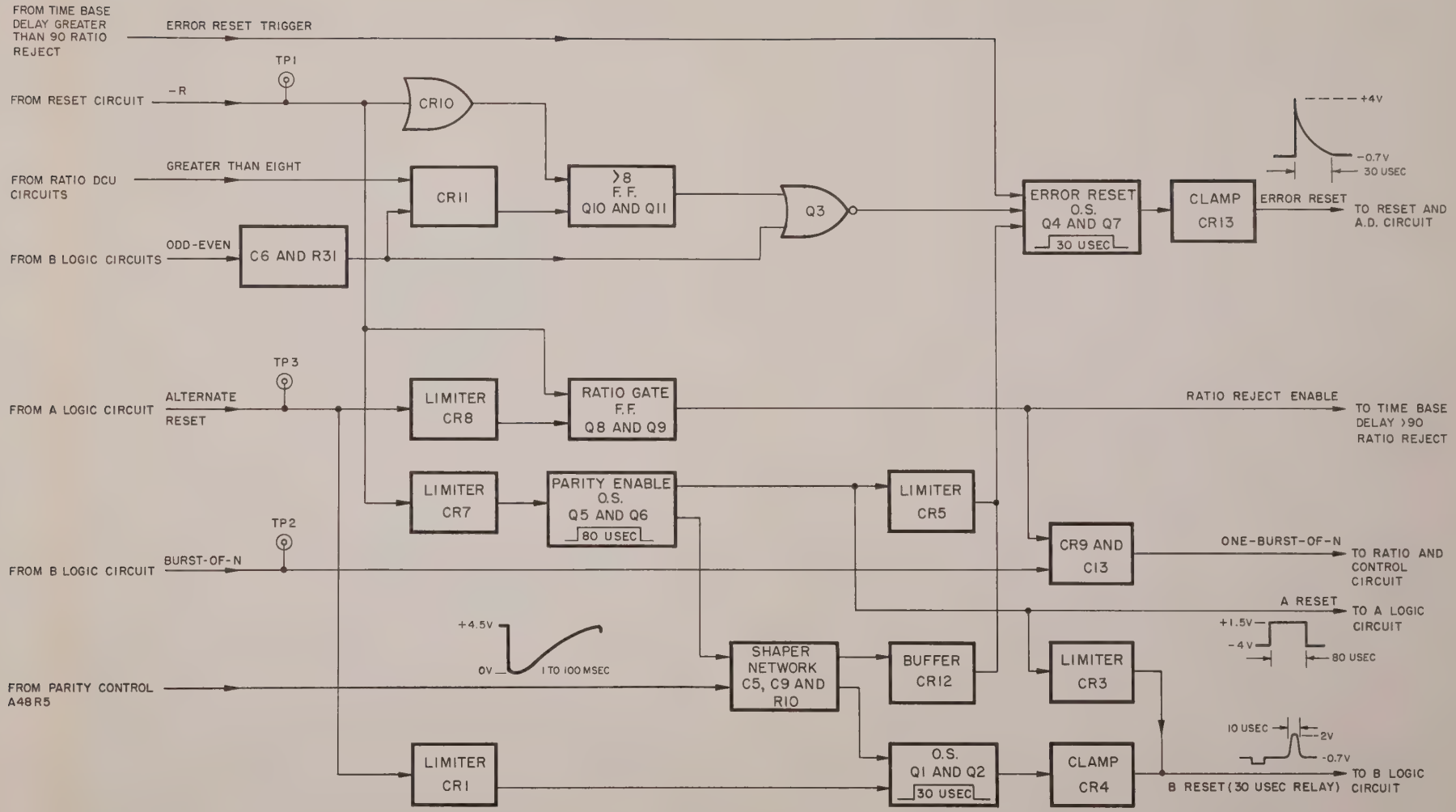


FIGURE 22. PARITY LOGIC CIRUIT BLOCK DIAGRAM

applied to an AND gate along with the parity enable pulse.

(3) The parity enable pulse is generated by the 80 microsecond one-shot flip-flop (transistors Q5 and Q6). Initially transistor Q6 is biased conducting. As the reset pulse occurs, transistor Q6 is cut off and the 80 microsecond pulse is generated. The transistor Q6 is coupled to transistor Q5 through resistor R14. Transistor Q5 now conducts causing the collector voltage level to drop to a low level and discharging capacitor C9 through transistor Q5. The resultant voltage change generates a pulse that is coupled to AND gate Q4 through resistor R10 and diode CR12, and is combined with the 30 microsecond delay pulse.

(4) The alternate reset pulse applied to the ratio gate flip-flop is also applied to the 30 microsecond delay pulse generator circuit Q2. The alternate reset pulse is differentiated by capacitor C1 and resistor R1, limited by diode CR1, and applied to the base of transistor Q2. Transistor Q2 is normally conducting. The alternate reset pulse cuts off transistor Q2. This causes a current change through resistor R8. Two pulses are generated at the collector of Q2. The pulses applied through capacitor C4 to clamp diode CR4 and AND gate diodes (CR3 and CR5) as a 30 microsecond delay pulse. The pulse is ANDed with the parity enable pulse from transistor Q6 and the output is applied to AND gate Q4. The 30 microsecond pulse is also applied to the B logic circuit as a reset pulse for the B logic circuit binaries.

(5) If an output is generated by OR gate Q3, this pulse is ANDed with the output from CR3 and CR5 AND gate. The resultant pulse generated is applied to OR gate Q7. The output pulse generated from transistor Q7 becomes the error reset pulse. The pulse is applied to the reset circuit and causes an interruption of a frequency computation as a consistency error exists.

s. Ratio and Control Circuit, (A36). The ratio and control circuit amplifies and shapes the 1-MHz crystal oscillator output into square pulses, develops the N-Ratio measurement, and generates the N-Timing gate pulse. A block diagram of the ratio and control circuit is shown in Figure 23.

(1) The 1-MHz signal is applied to the 1-MHz shaper circuit (Q1 and Q2) to develop the 1-MHz square pulses. The pulses are applied to the time base and delay (A37) circuits for gating to the time base decade divider. The 1-MHz clock pulses drive the time base circuits (decade dividers A42, A43 and A44 and gates Q3, Q4 and CR12). The clock signal is divided by 1000 in the three decade dividers to develop a 1-KHz pulse which is reapplied through OR gate Q4 to two additional decade dividers (A45 and A46).

(2) The nine-carry output from decade dividers A42 through A46 is applied to the nine-carry line input to the start-stop flip-flop circuits and provides the trigger pulse to the start flip-flop (Q8 and Q9).

(3) The one-burst-of-N input from the parity logic circuit is supplied to the OR gate Q3 with the 1-MHz pulses. Diode CR12 is enabled by the readout flip-flop (Q6 and Q7) to pass the 1-MHz pulses to gate Q4.

(4) After the reset pulse occurs, the readout flip-flop is reset so that transistor Q7 is conducting. The readout flip-flop is enabled and decade dividers A38 through A46 are cleared. The resultant high level at the collector of Q7 is applied to diodes CR12 and CR13 to inhibit their conduction. This action prevents the 1-MHz pulses from passing through the gates. The burst-of-N pulses are applied to the ratio counter (decade dividers A38 and A39). An error count is developed and applied to the readout flip-flop. As the reset pulse clears all circuits, the A42, A43, and A44 decade dividers of the time base commence dividing the 1-MHz pulses. The ratio counters output (A38 and A39), is then applied to the readout flip-flop to enable gate CR12. The resultant action allows a certain number of 1-MHz pulses to pass through gate Q3 into decade divider A45 and A46 between the 1-KHz pulses. Since decade dividers A45 and A46 are normally counting 1-KHz pulses, the 1-MHz pulses are made to occur between two 1-KHz pulses. This action sets a count into the two decade dividers which is an accumulation of 1KHz pulses from A44 and the added 1-MHz pulses gated through.

(5) As additional 1-KHz pulses are counted, the second nine-carry pulse is generated at a time interval that is related to the one-burst-of-N pulse. The second nine-carry pulse sets the stop flip-flop to end the N-Timing gate pulse interval. The first nine-carry pulse that occurs from the time base decade dividers A42, through A46 sets the start flip-flop and generation of the N-Timing gate pulse. The nine-carry pulse passes through AND gate A36CR4 and sets the start flip-flop Q8. The output AND gate CR6 and CR7 is inhibited until the start flip-flop is set. Setting the start flip-flop causes Q9 to inhibit AND gate CR4 but enable AND gate CR5. As the second nine-carry pulse is generated by the time base decade dividers A42 through A46, the stop flip-flop is set, thereby inhibiting diode A36CR6 in the output AND gate. This setting of the start-stop flip-flops and resultant enabling and inhibiting of the output AND gate causes the generation of the N-Timing gate pulse. The N-Timing gate pulse is then applied to the C.U. circuit input through emitter follower Q12.

t. Reset Circuit, (A35). The reset circuit generates reset pulses, a read pulse applied to the memory readout circuits, and the print command pulses required to operate an external digital recorder.

A block diagram and timing chart of the reset circuit is shown in Figure 24. The reset circuit consists of three individual circuit functions controlled by a unijunction one-shot multivibrator circuit. These are the display timer generator, the reset pulse one-shot generator and the read pulse one-shot generator. Operation of the display timer provides the primary trigger control to the reset and read one-

applied to an AND gate along with the parity enable pulse.

(3) The parity enable pulse is generated by the 80 microsecond one-shot flip-flop (transistors Q5 and Q6). Initially transistor Q6 is biased conducting. As the reset pulse occurs, transistor Q6 is cut off and the 80 microsecond pulse is generated. The transistor Q6 is coupled to transistor Q5 through resistor R14. Transistor Q5 now conducts causing the collector voltage level to drop to a low level and discharging capacitor C9 through transistor Q5. The resultant voltage change generates a pulse that is coupled to AND gate Q4 through resistor R10 and diode CR12, and is combined with the 30 microsecond delay pulse.

(4) The alternate reset pulse applied to the ratio gate flip-flop is also applied to the 30 microsecond delay pulse generator circuit Q2. The alternate reset pulse is differentiated by capacitor C1 and resistor R1, limited by diode CR1, and applied to the base of transistor Q2. Transistor Q2 is normally conducting. The alternate reset pulse cuts off transistor Q2. This causes a current change through resistor R8. Two pulses are generated at the collector of Q2. The pulses applied through capacitor C4 to clamp diode CR4 and AND gate diodes (CR3 and CR5) as a 30 microsecond delay pulse. The pulse is ANDed with the parity enable pulse from transistor Q6 and the output is applied to AND gate Q4. The 30 microsecond pulse is also applied to the B logic circuit as a reset pulse for the B logic circuit binaries.

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(2) The nine-carry output from decade dividers A42 through A46 is applied to the nine-carry line input to the start-stop flip-flop circuits and provides the trigger pulse to the start flip-flop (Q8 and Q9).

(3) The one-burst-of-N input from the parity logic circuit is supplied to the OR gate Q3 with the 1-MHz pulses. Diode CR12 is enabled by the readout flip-flop (Q6 and Q7) to pass the 1-MHz pulses to gate Q4.

(4) After the reset pulse occurs, the readout flip-flop is reset so that transistor Q7 is conducting. The readout flip-flop is enabled and decade dividers A38 through A46 are cleared. The resultant high level at the collector of Q7 is applied to diodes CR12 and CR13 to inhibit their conduction. This action prevents the 1-MHz pulses from passing through the gates. The burst-of-N pulses are applied to the ratio counter (decade dividers A38 and A39). An error count is developed and applied to the readout flip-flop. As the reset pulse clears all circuits, the A42, A43, and A44 decade dividers of the time base commence dividing the 1-MHz pulses. The ratio counters output (A38 and A39), is then applied to the readout flip-flop to enable gate CR12. The resultant action allows a certain number of 1-MHz pulses to pass through gate Q3 into decade divider A45 and A46 between the 1-KHz pulses. Since decade dividers A45 and A46 are normally counting 1-KHz pulses, the 1-MHz pulses are made to occur between two 1-KHz pulses. This action sets a count into the two decade dividers which is an accumulation of 1KHz pulses from A44 and the added 1-MHz pulses gated through.

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t. Reset Circuit, (A35). The reset circuit generates reset pulses, a read pulse applied to the memory readout circuits, and the print command pulses required to operate an external digital recorder.

A block diagram and timing chart of the reset circuit is shown in Figure 24. The reset circuit consists of three individual circuit functions controlled by a unijunction one-shot multivibrator circuit. These are the display timer generator, the reset pulse one-shot generator and the read pulse one-shot generator. Operation of the display timer provides the primary trigger control to the reset and read one-

applied to an AND gate along with the parity enable pulse.

(3) The parity enable pulse is generated by the 80 microsecond one-shot flip-flop (transistors Q5 and Q6). Initially transistor Q6 is biased conducting. As the reset pulse occurs, transistor Q6 is cut off and the 80 microsecond pulse is generated. The transistor Q6 is coupled to transistor Q5 through resistor R14. Transistor Q5 now conducts causing the collector voltage level to drop to a low level and discharging capacitor C9 through transistor Q5. The resultant voltage change generates a pulse that is coupled to AND gate Q4 through resistor R10 and diode CR12, and is combined with the 30 microsecond delay pulse.

(4) The alternate reset pulse applied to the ratio gate flip-flop is also applied to the 30 microsecond delay pulse generator circuit Q2. The alternate reset pulse is differentiated by capacitor C1 and resistor R1, limited by diode CR1, and applied to the base of transistor Q2. Transistor Q2 is normally conducting. The alternate reset pulse cuts off transistor Q2. This causes a current change through resistor R8. Two pulses are generated at the collector of Q2. The pulses applied through capacitor C4 to clamp diode CR4 and AND gate diodes (CR3 and CR5) as a 30 microsecond delay pulse. The pulse is ANDed with the parity enable pulse from transistor Q6 and the output is applied to AND gate Q4. The 30 microsecond pulse is also applied to the B logic circuit as a reset pulse for the B logic circuit binaries.

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(2) The nine-carry output from decade dividers A42 through A46 is applied to the nine-carry line input to the start-stop flip-flop circuits and provides the trigger pulse to the start flip-flop (Q8 and Q9).

(3) The one-burst-of-N input from the parity logic circuit is supplied to the OR gate Q3 with the 1-MHz pulses. Diode CR12 is enabled by the readout flip-flop (Q6 and Q7) to pass the 1-MHz pulses to gate Q4.

(4) After the reset pulse occurs, the readout flip-flop is reset so that transistor Q7 is conducting. The readout flip-flop is enabled and decade dividers A38 through A46 are cleared. The resultant high level at the collector of Q7 is applied to diodes CR12 and CR13 to inhibit their conduction. This action prevents the 1-MHz pulses from passing through the gates. The burst-of-N pulses are applied to the ratio counter (decade dividers A38 and A39). An error count is developed and applied to the readout flip-flop. As the reset pulse clears all circuits, the A42, A43, and A44 decade dividers of the time base commence dividing the 1-MHz pulses. The ratio counters output (A38 and A39), is then applied to the readout flip-flop to enable gate CR12. The resultant action allows a certain number of 1-MHz pulses to pass through gate Q3 into decade divider A45 and A46 between the 1-KHz pulses. Since decade dividers A45 and A46 are normally counting 1-KHz pulses, the 1-MHz pulses are made to occur between two 1-KHz pulses. This action sets a count into the two decade dividers which is an accumulation of 1KHz pulses from A44 and the added 1-MHz pulses gated through.

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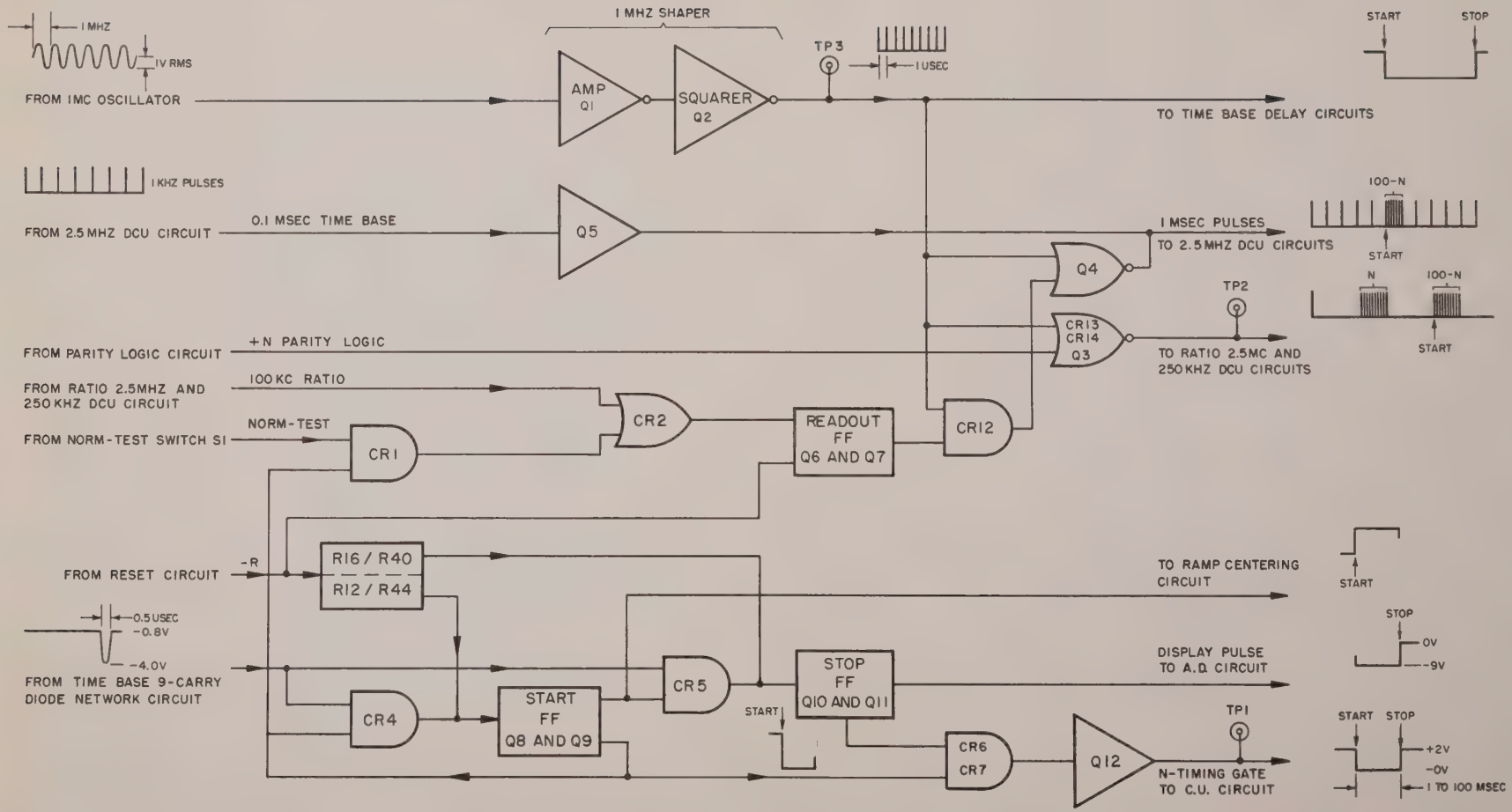


FIGURE 23. RATIO AND CONTROL CIRCUIT BLOCK DIAGRAM

shot multivibrators. Since all control functions are initially set by the reset pulse, this pulse is required to initiate the frequency measurement sequence.

The timing chart shows the time relationship of the following action. The nine-carry pulses (generated by the time base generator circuits) initiate the start-stop flip-flop action. At stop time a negative going display pulse is generated (by the stop-flip-flop A36Q10 and Q12) as shown in Figure 24. The leading edge of the display pulse initiates the resulting read, reset, and print commands.

(1) Display Timer Circuits. The display timer circuit, consisting of transistors Q1 through Q4, provide the timing control for each frequency measurement in the frequency counter. The operation of a unijunction transistor (Q3) provides the timing cycle that originates the trigger pulse applied to the reset one-shot multivibrator. The generation of the reset pulse is initiated by the application of the display pulse to transistor Q1. Transistors Q1 and Q2 form a trigger circuit and provide print command trigger pulses to an external mechanical printer. It also provides trigger pulses to the read one-shot multivibrator. Transistor Q1 is normally conducting. With Q1 on, Q3 is held off and the parallel timing capacitors C4 and C5 are in a neutral state (no charge). The negative going transition of the display pulse sets the trigger circuit Q1/Q2 by cutting off Q1. By reversing the conduction states of Q1 and Q2 the negative and positive print command pulses are generated in the respective collector circuits. Q2 provides a negative going print command and Q1 a positive. This positive signal from Q1 allows the timer capacitors (C4 and C5) to charge. This charge time is primarily the RC time of C4/C5 and R24 in series with the front panel display time control A48R43 and A48R44. An expotential voltage rise will be felt at the emitter of Q3. Also applied to the emitter are synchronizing pulses applied through Q4 from the F.S. circuit. The combined influence of the positive charge on C4/C5 and the sync pulses will bring Q3 into conduction. With the conduction of Q3 the capacitors C4/C5 are discharged and the negative going transition ends the display cycle. This results in a reset signal causing an end to the display pulse enabling the trigger circuit Q1/Q2, returning Q1 to the ON state, thus preventing Q3 from acting like a free running oscillator.

(2) Reset One-Shot. The reset one-shot multivibrator is normally biased with transistor Q7 off. The pulse supplied from transistor Q3 through capacitor C10 is a negative-going trigger pulse. This trigger pulse drives Q7 into conduction for the duration of the r-c time constant of capacitor C11 and resistor R31. The positive going 20 microsecond pulse, applied to the base of transistor Q9 by voltage divider resistors R32 and R33, is used to develop a negative going pulse at the collector of Q9. This pulse is applied as a negative going reset pulse throughout the instrument. A positive reset pulse is taken directly off the collector of Q7 and applied as required throughout the instrument.

(3) Secondary Reset Control. The reset one-shot may also be set by trigger pulses supplied through OR gates diodes CR6, CR8, CR9 and CR10. Capacitors C14, C16, and C17 that provide the inputs to the OR gates are biased to charge when one side of any one capacitor is grounded. The charging action of the capacitor causes a positive output pulse to be generated from the OR gate. The OR gate output is applied to the base of transistor Q8. Transistor Q8 is biased to conduct and the OR gate output causes the transistor to cutoff. The collector output from Q8 is coupled to the base of transistor Q7 through capacitor C11 and resistor R31. As transistor Q8 cuts off transistor Q7 conducts for the duration of the r-c time constant of C11 and R31. This results in the generation of the reset pulses.

(4) Read Pulse One-Shot. The read pulse applied to the memory readout circuits is generated by the read one-shot transistors Q5 and Q6. As the display pulse causes transistor Q1 to cutoff, Q2 comes into conduction. The voltage change in transistor Q2 collector output is applied to the read-one-shot multivibrator through capacitor C18 as a negative going trigger pulse. Transistor Q6 is normally biased conducting. The negative going trigger pulse causes the transistor to cutoff. The transistor is cutoff for the duration of the r-c time constant developed by capacitor C2 and resistors R5 and R7. This generates a 50 microsecond pulse. The pulse is then applied to the read amplifiers in the memory readout circuits to transfer the totalized N-Count set into the memory readout flip-flops.

(5) Read Pulse Secondary Control. The read one-shot may also be triggered by the error reset pulse generated in the parity logic circuit. The positive-going error reset pulse is coupled to the read one-shot multivibrator through capacitor C1 and buffer diode CR1. Transistor Q5 is biased at cutoff and the error reset pulse causes the transistor to conduct for the duration of the read pulse as described above.

(6) Print-Command Pulse Output. The print command pulses (+ and -) are generated by the display timer trigger circuit Q1 and Q2. The two amplifiers are in a normal quiescent state (Q1 conducting and Q2 cut off). Application of the display pulse to the base of Q1 causes Q1 to cut off and results in the generation of the print-command pulses. The two collector outputs are applied to an external digital recorder through the PRINT-OUT connector J22. The print command signals actuate the printer circuits when readout information is available.

u. Time Base Delay Circuit, (A37). The time base delay circuits perform three operational functions within the frequency counter. 1) To gate the clock signal to the time base decade counting chain, 2) to trigger the error reset circuitry, and 3) to produce the preset pulse for Option F. Each function is independent of the other and requires external signals for control. A block diagram of the time base delay circuits is shown in Figure 25.

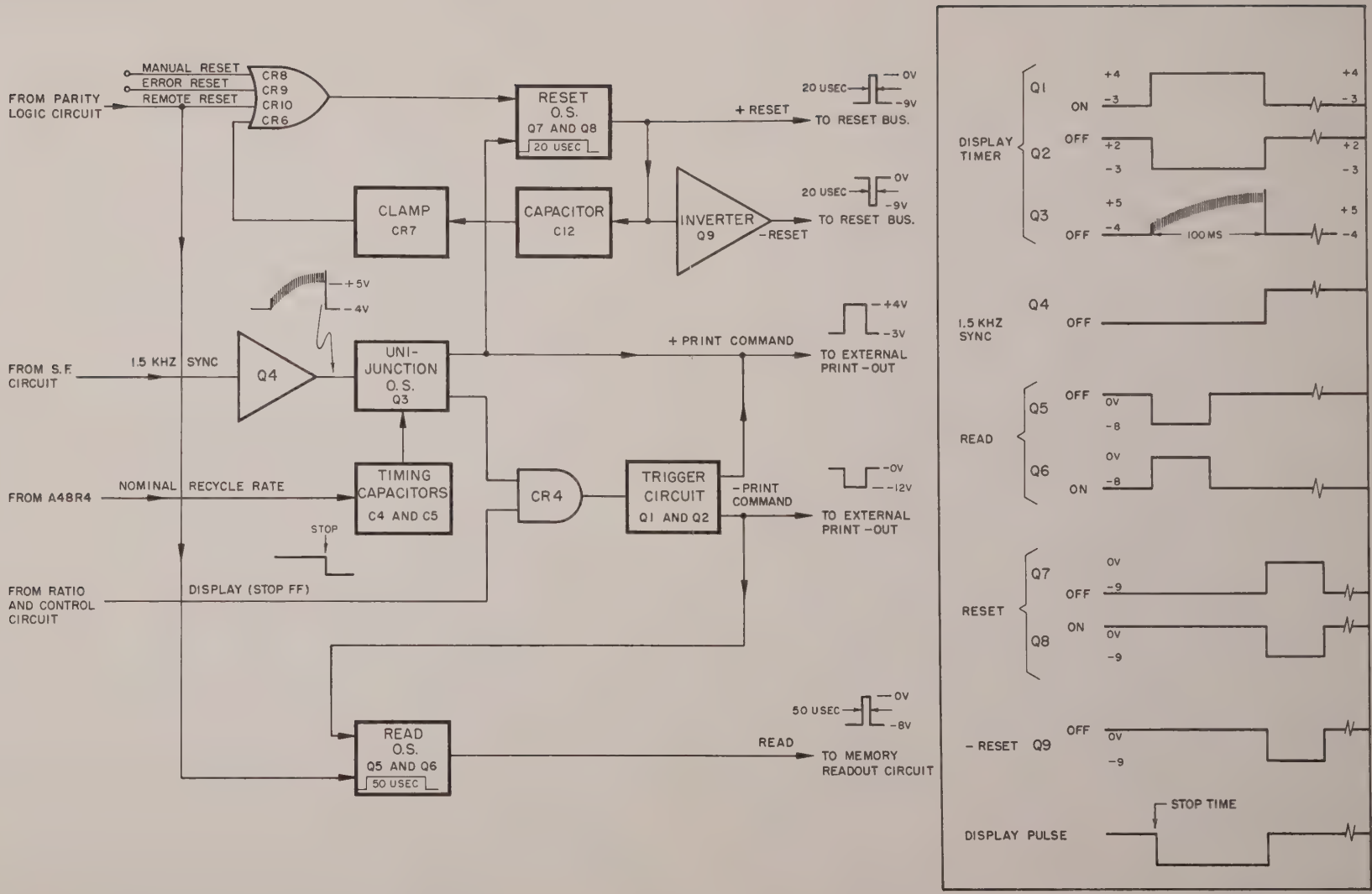


FIGURE 24. RESET CIRCUIT, BLOCK DIAGRAM AND TIMING FUNCTIONS

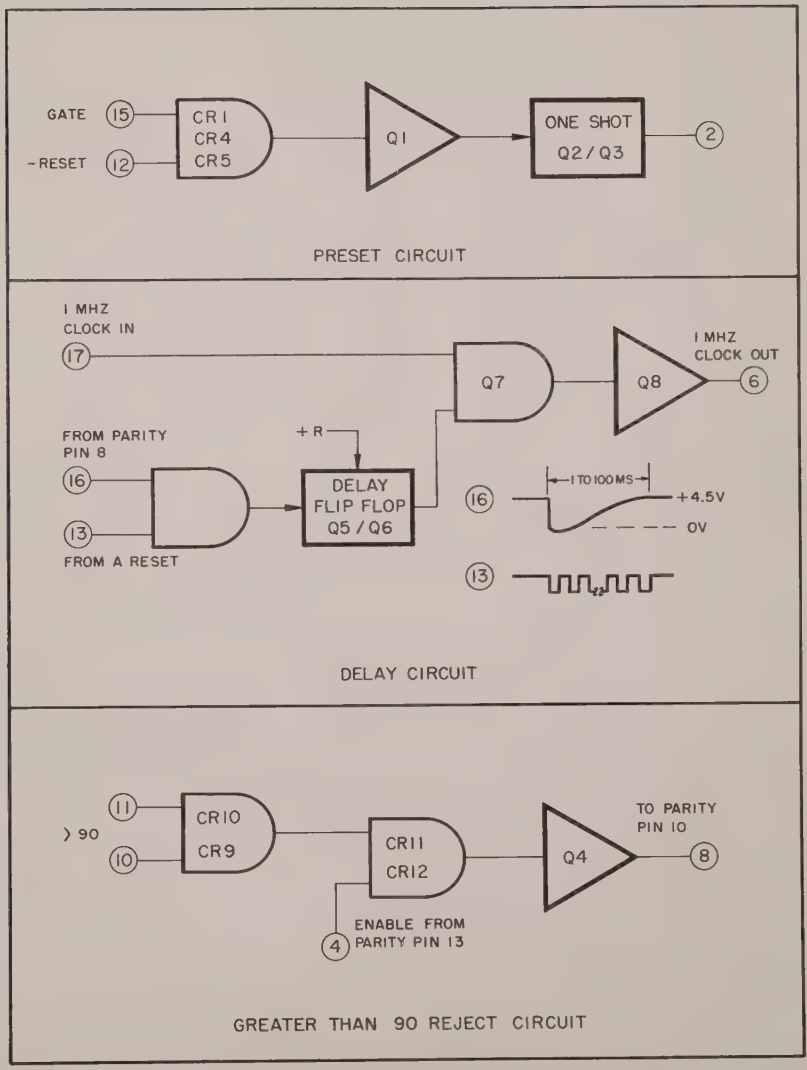


FIGURE 25. TIME BASE DELAY, BLOCK DIAGRAM

(1) Delay Function. The delay circuitry prevents the clock from driving the time base DCU's until after a parity check. The delay circuitry consists of the delay flip-flop Q5/Q6, gates CR15 and Q7 and the buffer amplifier Q8. The delay flip-flop is reset to a quiscent state with Q5 off and Q6 on. This allows Q7 to conduct, thereby clamping the clock input (at A37-17) to ground. With the delay flip-flop in the reset state A37-17 is grounded and the drive to the time base chain is grounded. When the parity enable pulse (A26-8) returns to a normal level in a time controlled by the front panel parity control (A48R5), Gate CR15 is enabled. On the next positive transition of the alternate reset pulse (A25-17) an input trigger is ANDed through CR15 to set the delay flip-flop. Setting Q5 on and Q6 off will reverse bias Q7 turning it off. With Q7 off the clock signal is coupled to the base of Q8 and drive to the time base chain is available at A37-6. In the Models 946/951 this signal is routed through the resolution switch (A48S6) to either A40, A41, A42, or A43 depending on the setting at A48S6. In the Models 945/950, A36-7 is connected directly to the input of A42.

(2) Greater than 90 Reject. If the N-Ratio signal into the ratio counter circuits (A38, A39) reaches a 90 count a trigger is generated producing an error reset generating a new measurement cycle. If the ratio counter has a greater than 90 count the input frequency is beyond the range selected. The greater-than-90-reject circuit consists of Amplifier Q4, Gates CR9/CR10 and CR11/CR12. When the ratio gate flip-flop in the parity logic (A26 Q8/Q9) is set Gate CR11/CR12 is enabled. The ratio counter circuits A38 and A39 count N-Ratio pulses. If a count of 90 is reached in A37 the 1 and 8 lines go true and a trigger is ANDed through CR9/CR10. This trigger is passed through Gate CR11/CR12 driving the amplifier Q4. This couples the signal to the error reset one-shot (A26 Q4/Q7) in the parity logic. Thus an error reset is produced generating a new measurement cycle.

(3) Preset Circuit. Option F, Remote Preset Reset standard in the Models 950/951 and an option in Models 945/946, utilizes this circuitry. The DCU's in the counting chain are normally reset to zero except when wired for an off-set reading as described under Option F. The trailing edge of the negative reset pulse is differentiated and applied to the Gate diodes CR1 and CR4. If A37-15 is enabled the positive transition will reverse bias CR7 and turn off Q1. This will trigger the one-shot Q2/Q3 producing a preset pulse at A37-2. The preset pulse is routed to the counting chain DCU's through the remote preset reset connector A49 J4.

v. Overflow Circuit, (A21). When seven digit instruments are equipped with Option F (Remote Preset Reset), the most significant digit is moved out one more place. This number can be preset to either one, two or three. A block diagram of the overflow circuit is shown in Figure 26. The overflow circuit consists of a pair of binaries Q1/Q2 and Q3/Q4, a pair of storage flip-flops Q5/Q6 and Q8/Q9, the buffer amplifiers Q7 and Q10 and the read gate Q11. A negative reset pulse is used to turn the number one and number two binaries to a reset condition which turns off the over-

flow indicators. An overflow from the 250 KHz decade counting unit (most significant digit) triggers the overflow circuits and sets the number one binary. On the next read pulse the number one storage flip-flop will be gated and a one condition will be transferred to the overflow light. This will cut off the buffer amplifier Q7 turning on the number one light. If two overflow pulses occur the number one binary will be returned to its reset state and produce a trigger pulse to set the number two binary. On the next read pulse the number two storage flip-flop will turn on the number two overflow light by cutting off Q10. If three inputs are counted within the overflow circuit both the number one and number two lights will be turned on. With Option F, the number one and two binaries can be programmed to cause the overflow lamps to remain on thus increasing by one digit the frequency readout display.

(1) Circuit operation begins with the reset pulse turning on Q2 and Q4 of the number one and two binaries respectively. This condition resets the storage flip-flops with Q6 and Q9 on. Buffer amplifiers Q7 and Q10 are therefore conducting and the overflow indicator lights are turned off. The read gate Q11 is held cut-off by the read pulse line.

(2) An overflow output from the 250 KHz decade counting unit will set the number one binary. On the next read pulse Q11 will conduct and transfer the one count into the number one storage flip-flop. Transferring a one into the storage flip-flop turns off Q6 and turns on Q5. This action will reverse bias Q7 and turn it off.

(3) Turning off Q7 allows the voltage level at the junction of terminal five to go positive. Terminal five is returned to the +300 volt supply through A48R8 on the front panel. The number one overflow light is also connected to this junction. Cutting off Q7 turns on the indicator light.

(4) If two overflow pulses occur the number one binary will be returned to a reset condition by the second overflow pulse. This will produce a carry pulse to the number two binary setting it. On the next read pulse Q11 will again gate the storage flip-flops. Since Q1 in the reset condition is cut off, Q6 of the number one storage flip-flop will be in the on state and no transfer will take place in this flip-flop. The number two binary is in the set state and therefore the read gate will set the number two storage flip-flop bringing Q8 into conduction and turning off Q9. This action will turn off Q10.

(5) Turning off Q10 allows the voltage at terminal six to go positive. Terminal six is returned to the +300 volt supply through A48R9 on the front panel. The number two overflow light is also connected to this junction. Cutting off Q10 turns on the number two indicator light.

(6) Either one or both of the overflow lamps can be turned on by wiring the remote preset reset connector A49J4 on the rear panel. This will cause the number one and/or the number two binaries to remain in a set condition. Thus the overflow lights will remain on.

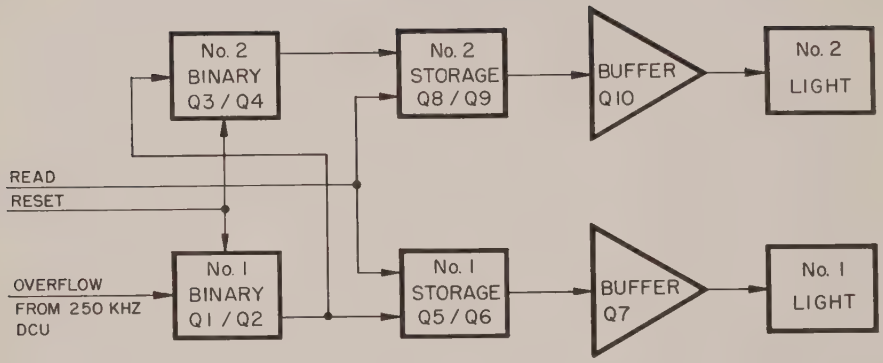


FIGURE 26. OVERFLOW CIRCUIT, BLOCK DIAGRAM

(7) If the reset has been programmed by Option F to reset to two an overflow will cause both the number one and number two binaries to be in a set condition. On the read pulse the number one and two storage flip-flops will be set turning on both the number one and two indicators.

(8) To wire the overflow lights to extend the frequency range (refer to Table 5) connect the pin corresponding to the overflow light to be turned on to pin 15 or 33 of the rear panel preset reset connector J4. This completes the loop between the number one or two light to the preset generator. Connect pin 18 to pin 34 on A49J4. This enables the preset generator input thereby turning on the indicator lamp.

w. Power Supply Circuit, (A47). The power supply circuit provides all the regulated and unregulated voltages used by the frequency counter. The power supply circuit develops the regulated ±12 and ±4.5 volts dc, the regulated +30 volts dc, and the unregulated +300 volts dc voltages. The power supply circuit chassis also is the mounting chassis for the power supply regulator printed circuit board connector and the chassis interconnection wiring. A block diagram of the power supply circuit with the associated power supply regulator is shown in Figure 27. The input ac power is supplied to the power supply circuit by setting the power switch (A48S1) to on. Any voltage transients in thepower line are filtered by the line filter (A49FL1). The filtered ac power is then applied to the primary winding of transformer A47T1. Four secondary windings are used to develop the dc voltage outputs.
CAUTION: Do not apply power to the power supply chassis if the power supply regulator is removed as damage to the instrument circuits may result.

(1) The ac output from a secondary winding is applied through a half-wave rectifier diode CR13 and filter network (C5, R44, and R45) to provide the unregulated +300 volt dc voltage. The +300 volts dc is then applied to the memory readout circuit to provide anode voltages for the numerical readouts.

(2) Another output from another secondary winding is applied through the full-wave rectifier diodes (CR14 and CR15) and the filter network (R47 and C6) to the power supply regulator circuit. The +38 volt dc output is regulated in the power supply regulator to develop the regulated +30 volts dc.

(3) The regulated ±12 volt dc voltages are developed from a third secondary winding output and applied to full-wave rectifier diodes CR6, CR16 (+12 vdc), CR7, and CR8 (-12 vdc). The +18 volt dc output from the diodes CR6 and CR16 is filtered by capacitor C3B and resistor R39. The filtered +18 volts dc is applied to the collector of series regulator Q3. The +12 volt regulator circuits provide the regulation control current to the base of regulator Q3. The regulated +12 volt dc output at transistor Q3 emitter is applied through fuse F4 to circuits in the frequency counter and also reapplied to the power supply regulator as the reference voltage for the ±12 and ±4.5 volt dc voltage regulator circuits. The -18 volt dc output from diodes CR7 and CR8 is filtered by capacitor C2 and R46 and applied to the collector of series regulator Q1. The -12 volt dc output at the emitter of the regulator is reapplied to the -12 volt regulator circuit as a reference voltage and through fuse F3 to circuits in the frequency counter.

(4) The regulated ±4.5 volt dc voltages are developed from a fourth secondary winding output and applied to full-wave rectifier diodes CR9, CR10 (+4.5 vdc) CR11, and CR12 (-4.5 vdc). The +8 volt dc output from diodes CR9 and CR10 is filtered by capacitor C3A and resistor R41 and applied to the collector of series regulator Q4. The regulated +4.5 volt dc output at regulator Q4 emitter is reapplied to the power supply regulator circuit as the output reference voltage for the +4.5 voltage regulator and through fuse F2 to circuits in the frequency counter. The -8 volt dc output from diodes CR11 and CR12 is filtered by capacitor C1 and resistor R42 and applied to the collector of series regulator Q2. The regulated -4.5 volt dc output at regulator Q2 emitter is reapplied to the -4.5 volt regulator circuit as a reference voltage and through fuse F1 to circuits in the frequency counter.

x. Power Supply Regulator Circuits, (A47A1). The power supply regulator circuits provide the +30, ±12, and ±4.5 voltage regulation controlling functions for the dc power supply. A block diagram of the power supply regulator circuits is shown in Figure 27. The power supply regulator is mounted on the power supply chassis.

(1) The unregulated +38 volts dc supplied by the power supply is applied to the collector of series regulator Q5, to the base of the regulator and to the anode of 30 volt reference diode through resistor RX. The voltage level at the junction of the resistor and diode serves as a voltage reference to prevent the voltage applied to the base of the regulator from rising above 30 volts. If the emitter output from the regulator drops lower than 30 volts the regulator increases conduction to readjust the emitter output to 30 volts dc. The 30 volt dc output at the regulator emitter is filtered by capacitor C15 and applied to the printed circuit board connector and to the +12 volt dc regulator circuit.

(2) The unregulated +18 volts dc supplied by the power supply to the +12 volt series regulator is also applied to the collector of regulator driver Q4. The regulated output from the series regulator is reapplied to the power supply regulator across voltage divider resistors R19, R20, and R21. Resistor R19 is a low resistance value and paralleled with the +12 ADJ control R4. Any voltage change in the voltage divider network is also reflected across the +12 ADJ control which is direct coupled to the base of the error reference amplifier Q2. Transistor Q2 is emitter-to emitter coupled to reference amplifier Q1 to form a differential amplifier circuit. Any change in current flow in either half of the differential amplifier will be reflected on the other half of the circuit. The error reference amplifier output is direct-coupled through current amplifiers Q3 and regulator driver Q4 to the base of series regulator Q3 in the power supply. Since diode CR2 will retain the reference amplifier base at a constant voltage level, (5.1 volts), any change of voltage applied to the collector or any change in the voltage drop across the voltage divider network, causes a resultant readjustment in conduction of the series regulator output.

(3) The regulated -12 volt dc circuit functions in a similar manner as the +12 volt circuit. The regulated +12 volts dc is applied across -12 ADJ voltage divider R7, R8 and R14. The -12 ADJ control is paralleled across R8 to permit a fine adjustment of any voltage drop in thevoltage divider network. The -12 ADJ control output is amplified by error amplifier Q6 and applied to the series regulator A47Q1 in thepower supply through amplifier Q7 and regulator driver Q8. Any change in the voltage drop across the voltage divider network causes a resultant readjustment in conduction of the series regulator to change the regulator emitter output.

(4) The ±4.5 volt dc regulator circuits are similar to the -12 volt dc regulator circuit and functions in a similar manner. The error reference voltage developed in a voltage divider and the +4.5 ADJ and -4.5 ADJ controls outputs are amplified and applied to series regulators in the power supply. The resultant change in the series regulator outputs is fed back to the individual voltage divider network which results in correcting the regulator output.

y. One-Megahertz Oscillator Circuit, (A47Y1). The 1-MHz oscillator circuit generates a stable one megahertz frequency that serves as the time base generator circuit reference source for all frequency measurements. The oscillator assembly is a thermally insulated chamber which contains a heating element, a temperature sensing circuit, an extremely stable one megahertz piezo-electric crystal, and the associated oscillator circuit components. The 1-MHz oscillator output is applied to the ratio and control circuit where amplifying and shaping (A37Q1 and A37Q2) is performed to supply one microsecond pulses to the time base generator circuits for scaling and trigger control. Provisions are made to bypass the internal oscillator output and permit the use of an external one megahertz oscillator frequency.

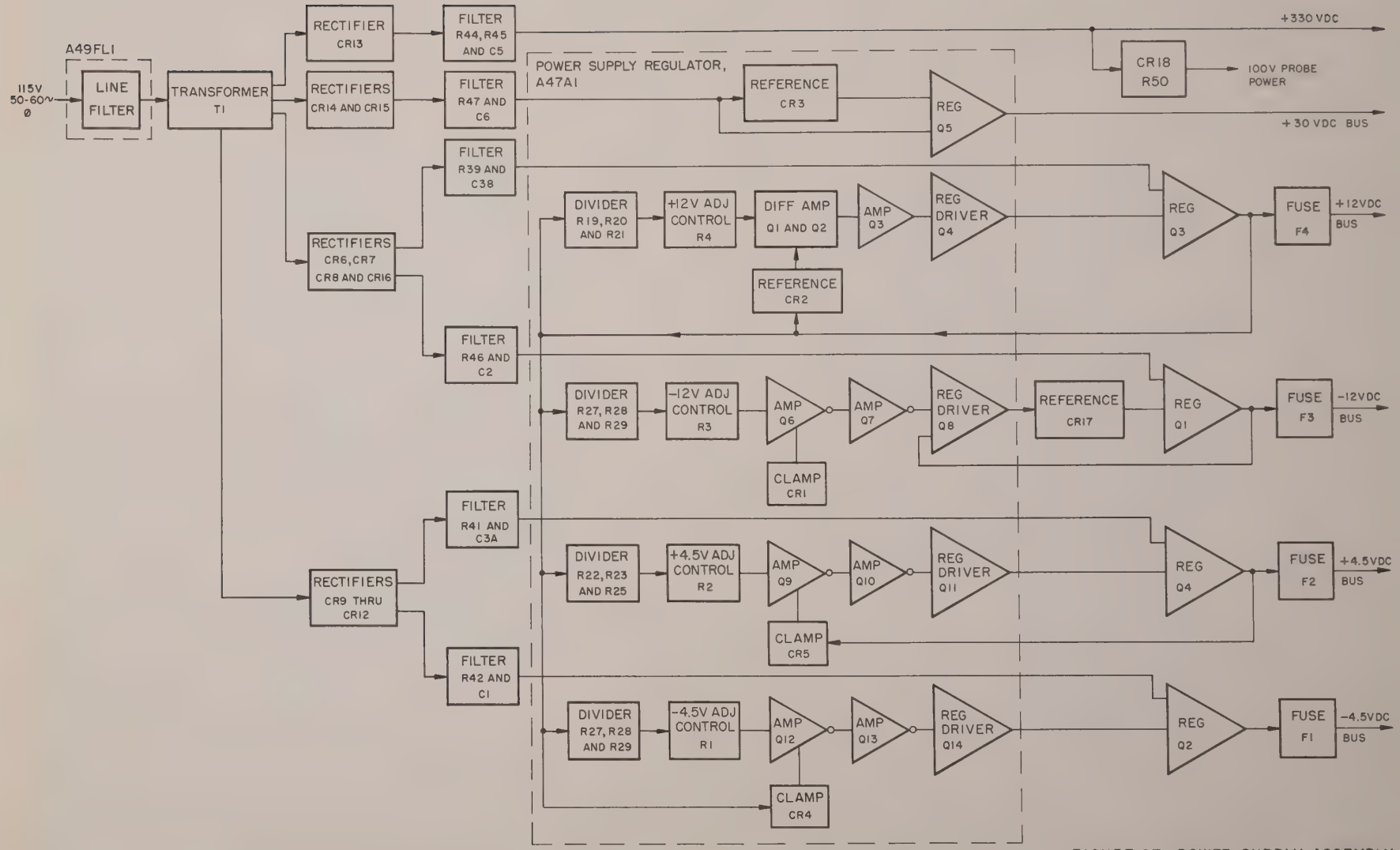


FIGURE 27. POWER SUPPLY ASSEMBLY BLOCK DIAGRAM

Chapter 5

MAINTENANCE

Section I PREVENTIVE MAINTENANCE

29. GENERAL

This section provides maintenance and troubleshooting information for the frequency counter. Included are periodic preventive maintenance checks, a performance checkout procedure, troubleshooting procedures, and repair and adjustment procedures.

30. PREVENTIVE MAINTENANCE

Preventive Maintenance is the systematic care, servicing, and inspection of equipment to prevent the occurance of trouble, to reduce down time, and to assure that the equipment is servicable. The preventive maintenance checks and service charts outline checks and services to be performed at a specific interval. These checks and services are to maintain electronic equipment in a servicable condition. To assist operators in maintaining servicability, the charts indicate what to check, how to check, and what the normal conditions are. The References column in the table lists the illustrations or paragraphs that contain detailed repair or replacement procedures.

31. PREVENTIVE MAINTENANCE CHECKS

Preventive Maintenance Checks of the frequency counter are required daily and monthly.

a. Daily Preventive Maintenance Checks. The Daily Preventive Maintenance Checks are listed in Table 9.

b. Monthly Preventive Maintenance Checks. The Monthly Preventive Maintenance Checks are listed in Table 10.

32. CLEANING OF THE FREQUENCY COUNTER.

Clean the equipment by brushing, wiping with a lintfree cloth, vacuuming, or by blowing with compressed air. Solvents may be used when specified for additional cleaning action. Use brush or cloth moistened with solvent to clean dirty portions of the instrument. The following materials, or their equivalent, are used for maintenance.

Lintfree cloth
Stiff (non-metallic) bristle brush
Solvent (Alcohol and water 50/50)
R. P. Filter coat
Compressed Air (filtered, moisture-and-oil-free, 30 psi maximum)
60/40 Solder
Warning: When using solvents provide adequate ventilation and skin protection.

Caution: Solvents may damage paint and identification marks.

Note: Frequent cleansing of the air filter element may be required when the instrument is operated in unusually severe environments.

Table 9. Daily Preventive Maintenance Checks

Sequence No.	Item	Procedure
1.	Connectors	Check the tightness of all external connectors.
2.	Controls & Indicators	While making the operating checks, observe that the mechanical action of each switch is smooth and free of external or internal binding and no excessive looseness is apparent.
3.	Reference Oscillator Frequency	Check 1 MHz output with frequency standard. Refer to Table 12.
4.	Air Filter	Check for unobstructed air flow and blower operation.

Table 10. Monthly Preventive Maintenance Checks

Sequence No.	Item	Procedure
1.	Pluckout items	Inspect pluckout item seating. Make certain that 1-MHz oscillator base clamp grips base securely.
2.	Jacks	Inspect Jacks for snug fit and good contact.
3.	Transformer	Inspect the leads on the power transformer. All mounting nuts must be tight. No dirt, corrosion or oil should be evident.
4.	Terminal Blocks	Inspect terminal blocks for loose connections and cracked or broken insulation.
5.	Air Filter	Inspect the air filter on the blower fan assembly. No dirt or corrosion should be evident.
6.	Cables	Inspect cords, cables, and wires for chafed, cracked or frayed insulation. Replace connectors that are broken, arced, stripped or worn excessively.
7.	Handle	Inspect handles for looseness - Replace or tighten as necessary.
8.	Metal Surfaces	Inspect exposed metal surfaces for rust and corrosion. Clean and touch up paint as required.
9.	Overall Performance Check.	Observe frequency readout in mid and high band range settings. Refer to Table 12.

33. GENERAL

This section contains procedures for performance checks of the frequency counter. These procedures are arranged to assist in locating a defective stage or circuit board that may not be functioning correctly during the performance check. Wherever possible, printed circuit boards and circuit assemblies are checked while operating in the instrument. This assures actual operating conditions and permits making performance checks with a minimum of external equipment.

34. TEST EQUIPMENT REQUIRED

Recommended test equipment for performance checks is listed in Table 11. Test equipment other than those listed may be used if their specifications equal or exceed the required test equipment specifications.

Cautions:

1. This equipment contains transistor circuits. If any equipment item does not have an isolation transformer in its power supply circuit, connect one in the power input circuit.

2. Never connect test equipment (other than oscilloscopes, multimeters, and vtvm's) outputs directly to a transistor circuit; use a coupling capacitor.

3. Make test equipment connections with care so that shorts will not be caused by exposed test equipment connectors. When making contact to the circuit under test, tape or sleeve (spaghetti) test prods or clips to leave as little area exposed as possible to minimize inadvertant shorts.

4. The equipment must be turned off before removing a printed circuit board. The transient voltages, created by board removal, may exceed the punch-through rating of the transistors.

35. TEST EQUIPMENT, TOOLS, AND MATERIALS

All test equipment required to perform the procedures given in this section are listed in Table 11. No special tools or materials are required.

Table 11. Test Equipment

Nomenclature	Model or Equivalent
Digital Electronic Voltmeter	HP 405
Oscilloscope	Tektronix 581 dc to 85 MHz
Oscilloscope	Tektronix 585 with type 82 plug-in.
LF Signal Generator	HP 202C, 1Hz to 100 Hz
HF Signal Generator	HP 606A, 50 Hz to 65 MHz
VHF Signal Generator	HP 608C, 10 to 480 MHz
UHF Signal Generator	HP 612A, 450 to 1230 MHz
UHF Signal Generator	HP 614A, 800 to 2100 MHz
UHF Signal Generator	HP 616, 1.8 to 4.2 GHz
SHF Signal Generator	HP 618, 3.8 to 7.6 GHz

36. PERFORMANCE CHECKOUT PROCEDURE

The performance checkout is used to determine if the frequency counter is functioning correctly. If a digital recorder is connected to the instrument, all frequency indications will automatically be recorded.

Table 12. Performance Checkout Procedure Chart

Step No.	Test Equipment Control Settings	Equipment Under Test Control Settings	Test Procedure	Performance Standard
1	Standard oscilloscope settings for Lissajous Test Patterns	Turn instrument on. Check that 1 MHz INT-EXT switch is in the **INT** position.	Reference Oscillator Frequency Check. Connect External 1 MHz Frequency standard to the oscilloscope horizontal input. Connect 1 MHz monitor output jack A49J1 to the oscilloscope vertical input. Adjust Trimmer (top center) on reference crystal A47Y1 for a circle on the oscilloscope face.	1:1 Ratio Lissajous Pattern
2	None		Overall performance check.	
		a. Remove external frequency input to A48Z1. b. Turn instrument on. c. Position S1 Test Normal Switch (left side panel) to the Test (T) position. d. Parity to minimum (ccw) e. Trigger switch to Manual (Option A). f. Trigger Control minimum (ccw). g. Display switch to store. h. Display time to minimum (ccw) i. Range switch to Mid band position.	a. Observe frequency readout at the low end (ccw) of trigger control, reading should be approximately b. Rotate trigger control slowly (cw) and observe the frequency readout. Frequency should increase in count sequentially without reading zeros. At maximum (cw) setting reading should be approximately	8.75 MHz ±1 MHz 10.1 MHz ±1 MHz
3	None	All settings as in step 2 except Range switch to High band setting.	a. Observe frequency readout at the low end of trigger control (ccw) frequency should be.....	71MHz ±1MHz

Table 12. Performance Checkout Procedure Chart (Con't)

Step No.	Test Equipment Control Settings	Equipment Under Test Control Settings	Test Procedure	Performance Standard
			b. Rotate Trigger control slowly (cw) and observe the frequency readout. Frequency should increase in count sequentially without reading zeros. At maximum (cw) setting reading should be.....	82MHz ±1MHz
4	None	Models 950/951 and instruments with Option F.	Preset Check	
		Fabricate Amphenol Connector 57-30360 to preset counter to read all sevens.	Connect fabricated Connector to A48J4	Frequency Display should readout 7777.700 MHz on Model 950 and 777777.700 MHz on Model 951.
5	None	Models 950/951 and instruments with Option F.		
		Fabricate Amphenol connector 57-30360 to preset counter to read all nines. See Table 5.	Connect fabricated connector to A48J4.	Frequency display should readout 9999.900MHz on Model 950 and 999999.900 MHz on Model 951.
6		Turn instrument on.	Power Supply Check.	
			a. Measure AC line voltage line voltage should be between	90 & 135 volts

ORIGINAL

Table 12. Performance Checkout Procedure Chart (Con't)

Step No.	Test Equipment Control Settings	Equipment Under Test Control Settings	Test Procedure	Performance Standard
			b. Measure power supply regulated and unregulated voltages. Voltage readings should be	+12 volts ±.12 +4.5 volts ±.045 -12 volts ±.12 -4.5 volts ±.045 +30 volts ±.3 +100 volts ±1 +300 volts +125 -60
7			Power Supply Ripple Check.	
	Calibrate oscilloscope to a 1 or 2 volt signal. Use plug-in with 5mv/cm sensitivity or better.	Turn instrument on. Ac line voltage should be nominal 115 volts.	a. Connect oscilloscope to the regulated +12 volt output (C4B is a convenient point). Observe peak to peak ripple voltage. Ripple should be less than	5 mv
			b. Connect oscilloscope to the regulated +4.5 volt output (C4A is a convenient point). Observe peak to peak ripple voltage. Ripple should be less than	5 mv
			c. Connect oscilloscope to the regulated -12 volt output, (C7 is a convenient point). Observe peak to peak ripple voltage. Ripple should be less than	5 mv
			d. Connect oscilloscope to the regulated -4.5 volt output, (C8 is a convenient point). Observe	

Table 12. Performance Checkout Procedure Chart (Con't)

Step No.	Test Equipment Control Settings	Equipment Under Test Control Settings	Test Procedure	Performance Standard
			d. (cont.) peak to peak ripple voltage. Ripple should be less than	5 mv
			e. Connect oscilloscope to the regulated +30 volt output (A47J1-15 is a convenient point). Observe peak to peak ripple voltage. Ripple should be less than	100 mv
		Instruments with Option P.	f. Connect oscilloscope to the regulated +100 volt output (junction at A47R50 and A47CR18 is a convenient point). Observe peak to peak ripple voltage. Ripple should be less than	300 mv
	Calibrate oscilloscope to a 10 volt signal		g. Connect oscilloscope to the +300 volt output (C5A is a convenient point). Observe peak to peak ripple voltage. Ripple should be less than	5 v

ORIGINAL

37. GENERAL

Troubleshooting of the frequency counter is based upon the performance checks. Maintenance troubleshooting procedures normally will be limited to the repair of parts and the replacement of printed circuit boards. This section includes troubleshooting information necessary to determine the nature of the repair required, disassembly and assembly techniques necessary to effect the repair, and all testing procedures needed to assure serviceability of repaired items.

38. TROUBLESHOOTING

To troubleshoot the instrument, perform the steps indicated in the troubleshooting chart Table 13. Perform all functions listed proceeding through the steps until an abnormal condition or result is observed. Schematic diagrams are included at the rear of this section. Part location illustrations are included in Chapter 8. It is strongly recommended that repair personnel observe waveforms at the various key points throughout the instrument (particularly the input sampler circuits) when the instrument is known to be operating normally. These waveforms should be observed under different operating modes and at different frequencies and their differences noted. In this way when the instrument is defective the troubleshooter is prepared to detect a faulty waveform.

NOTE: This does not imply indiscriminate probing within the circuits or adjusting any internal controls as serious missalignment can result.

39. TROUBLESHOOTING PROCEDURES

a. General. The first step in servicing a defective frequency counter is to sectionalize the fault. Sectionalization means tracing the fault to a unit such as the power supply. The second step is to localize the fault. Localization means tracing the fault to a defective stage or circuit responsible for the abnormal condition. The third step is isolation. Isolation means the locating of the defective part or parts. Some defective parts, such as burned resistors and arcing shorted transformers can often be located by sight, smell, and hearing. Most defective parts, however, must be isolated by checking voltages and resistance.

b. Sectionalization. The frequency counter consists of a single unit with numerous separate sub-assemblies. The first step in tracing trouble is to locate the sub-assembly at fault by the following methods:

(1) Visual Inspection. The purpose of visual inspection is to locate faults without testing or measuring circuits. All meter readings or other visual signs should be observed and an attempt made to sectionalize the fault to a particular unit.

(2) Operational tests. Operational tests frequently indicate the general location of trouble. In many instances, the tests will help in determining the exact nature of the fault. If the exact nature of the instrument malfunction is not known, perform the performance checkout procedures first.

c. Localization. Localization procedures should be performed after the trouble has been sectionalized (b above). The localization procedures applicable to this equipment are listed in (1) below, and should be used in localizing the trouble to a stage or module in the suspected unit.

(1) Troubleshooting Chart. The troubleshooting chart, Table 13, lists symptoms of common troubles and gives (or references) corrective measures. Such a chart obviously cannot include all trouble symptoms that may occur. The repairman should use this chart as a guide in analyzing symptoms that may not be listed.

d. Techniques. In performing the sectionalization, localization, and isolation procedures, one or more of the techniques below may be applied. Apply these techniques only as indicated, and observe all cautions.

(1) Voltage measurements. This equipment is transistorized. When measuring voltages, use tape or sleeving (spaghetti) to insulate the entire test prod, except for the extreme tip. A momentary short can ruin a transistor.

(2) Waveforms Analysis.

(a) Waveforms may be observed at various test points and connector pins in the circuits of the frequency counter. The normal waveforms obtained are shown in Chapter 4. on the applicable block diagrams and timing diagrams. By comparing the ideal observed waveforms with the normal waveforms, a malfunction sometimes will be isolated and located.

(b) A departure from the normal waveform indicates trouble between the point at which the waveform is observed to be normal and the point at which the waveform is observed to be abnormal. For example, if a waveform is observed to be normal at the base of a stage, and abnormal at the collector or output of the same stage, it is an indication that trouble is in that stage.

(c) When trouble is indicated in a stage, check any other inputs to the printed circuit board to determine the first malfunction indication is not a result of a malfunction supplied by a second circuit. If all other inputs are normal, replace the printed circuit board before making any further tests. If replacing the printed circuit board does not correct the trouble, place the original printed circuit board back in the connector and take voltage and resistance measurements at the connector socket.

(d) Various printed circuit baords may be interchanged, however, only with like type boards. Printed circuit boards in the time base circuits or decade counting unit are interchangeable with the same part number printed circuit boards. If the board is interchanged with a similar function but not the same part number (a 2.5 MHz DCU and a 250 KHz DCU), some change in performance will occur.

(e) When a waveform at a certain point is observed to be abnormal, the cause may be the absence of a signal from another unit. The point to start checking waveforms is at the unit input connector.

(e) (Cont.)

CAUTION: Before using any ohmmeter to test transistors or transistor circuits, check the open-circuit voltage across the ohmmeter test leads. Do not use the ohmmeter if the open-circuit voltage exceeds 1.5 volts. Also, since the Rx1 range normally connects the ohmmeter internal battery directly across the test leads, the comparatively high current (50 ma or more) may damage the transistor under test. As a general rule, the Rx1 range of any ohmmeter should not be used when testing low-powered transistors.

(3) Test Points. Generally boards are equipped with test jacks to facilitate connection of test equipment to various units. The test points should be used whenever possible to avoid needless disassembly of the equipment. These test points are shown on the printed circuit board schematic diagrams (Figures 28 through 42) and on the parts location diagrams in Chapter 7.

(4) Intermittent Troubles. In all the tests, the possibility of intermittent troubles should not be overlooked. If present, this type of trouble often may be made to appear by tapping or gently jarring the equipment. Make a visual inspection of all wiring and connections. Minute cracks in printed circuit boards can cause intermittent operation. A magnifying glass is often helpful in locating defects in printed boards. Continuity measurements of printed conductors may be made using the same technique ordinarily used on hidden conventional wiring.

40. LOCALIZING TROUBLES

a. General. In the troubleshooting chart procedures are outlined for sectionalizing troubles to the power supply or to the frequency measuring circuits and for localizing troubles to a stage within the various sections of the instrument. Depending on the nature of the operational symptoms, one or more of the localizing procedures will be necessary. When trouble has been localized to a particular stage, use voltage and resistance measurements to isolate the trouble to a particular part.

b. Use of Chart. When an abnormal symptom has been observed in the equipment, look for a description of this symptom in the Symptom column and perform the corrective measure shown in the Checks and Corrective Measures column.

c. Conditions for Tests. All checks outlined in the chart are to be conducted with the frequency counter connected to a power source as described in paragraph 41.

41. TEST SETUP

Bench tests of the frequency counter requires connections to a power source and to various test equipments. The power source must be connected to the frequency counter for all dynamic-servicing procedures. The test equipment use will vary with input frequency covered. Remove the top and bottom covers and make a test setup as outlined below:

CAUTION: Before making the connections observe the cautions in paragraph 34. Transistor damage may be avoided.

(1) Disconnect the power and signal input cables.

(2) Remove the instrument from the operating bench or mounting rack and place on a convenient work bench in a repair area.

(3) Remove the covers as follows:

(a) Twist the locking screws mounted around the cover edge 1/4 turn counterclockwise to release the top cover.

(b) The bottom cover is removed in a similar manner, twisting each screw 1/4 turn counterclockwise to release the bottom cover.

(c) The top and bottom covers are installed by placing the individual cover over the mounting area and while gently pressing the cover in place, setting each screw with a 1/4 turn, in a clockwise direction to lock in position.

NOTE: If the instrument is shielded for radio frequency interference (Option I, RFI), make sure the covers are seated properly to prevent any radiation of spurious radio frequency interference signals.

(4) Make sure the POWER switch is in the OFF position. Connect the instrument to a convenient power source for use in bench tests.

(5) Perform the Troubleshooting Procedures in Table 13.

Table 13. Troubleshooting Chart

Step	Symptom	Probable trouble	Check and Corrective Measures
1.	Readout indicators do not light, decimal lamp does not light, blower fan does not operate.	a. Power cable loose.	Tighten power cable and check for 115 volts ac. Pins 1 and 6 of the oscillator socket is a convenient point. Pins 3 and 8 on Option D instruments.
		b. Line fuse defective.	Replace defective fuse A49F1.
		c. POWER switch defective.	Replace defective switch A48S1.
		d. Blower fan defective	Replace defective blower fan A49B1 (paragraph 44 i).
2.	Readout indicators do not light.	a. Defective +330 volt dc power supply. circuit.	Troubleshoot and repair +330 volt power supply circuit.
3.	A readout indicator does not light or is blinking erratically when POWER switch is set to ON.	a. Memory readout circuit defective.	Troubleshoot and replace defective memory readout circuit.
4.	Absence of +12 volt dc or out of tolerance.	a. Defective +12 volt dc circuit.	Check +12 ±0.12 volts dc at fuse A47F4; check +12 volts dc circuit calibration (paragraph 48).
		b. Power supply regulator defective*	Check and replace defective power supply regulator A47A1.
5.	Absence of -12 volts dc or out of tolerance.	a. Defective -12 volts dc circuit.	Check for -12 ±0.12 volts dc at fuse A47F3; check -12 volts dc circuit calibration (paragraph 48).
		b. Power supply regulator defective.	Check and replace defective power supply regulator A47A1.

* Power should not be applied to an instrument with the regulator card removed or if it has defective circuitry.

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable trouble	Checks and Corrective Measures
6.	Absence of +4.5 volts dc or out of tolerance.	a. Defective +4.5 volts dc circuit.	Check for +4.5 ±0.045 volts dc at fuse A47F2. Check +4.5 volts dc circuit calibration (paragraph 48).
		b. Power supply regulator defective.	Check and replace defective power supply regulator A47A1.
7.	Absence of -4.5 volts dc or out of tolerance.	a. Defective -4.5 volts dc circuit.	Check for -4.5 ±0.045 volts dc at fuse A47F1. Check -4.5 volts dc circuit calibration (paragraph 48).
		b. Power supply regulator defective.	Check and replace defective power supply regulator A47A1.
8.	Absence of +30 volts dc or out of tolerance.	a. Defective +30 volts dc circuit.	Check for +30 ±0.3 volts dc at pin 12 of A47A1.
		b. Defective power supply regulator.	Check and replace defective power supply regulator A47A1.
9.	Any one readout indicator defective; decimal lamp lights.	The associated memory readout circuit defective.	Replace memory readout A10, A12, A14, A16, A18 or A20 (paragraph 44 c.). Check the associated counter unit.
		Defective indicator tube.	Replace indicator tube.
10.	Readout indicator lights but does not index.	Defective counter unit.	Check and replace defective counter unit A13, A16, A17, A19 or A21.
11.	Readout indication frequency measurement slightly inaccurate.	1-MHz oscillator defective or out of tolerance.	Check for 1.0 MHz ±20 Hz at A49J3 with an electronic counter. If out of tolerance, perform calibration procedure paragraph 46.
12.	Absence of 1-MHz oscillator output at A49J3 or out of tolerance. If oscillator is inoperative instrument will not function in any way.	a. Defective 1-MHz oscillator.	Check 1-MHz oscillator calibration (paragraph 46).
		b. Defect +12 volts dc circuit.	Check and repair +12 volt dc circuit.

ORIGINAL

ORIGINAL

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable trouble	Checks and Corrective Measures
13.	Readout indication repeated measurement error indication.*	Insufficient input signal.	Check and adjust input signal for 1 volt rms maximum. Unless otherwise noted an external frequency source should be applied to the input and the range switch set accordingly.
14.	Display indicator functions on low band but repeated measurement error indication on other channels.	a. Repeat step 13.	Repeat step 13.
		b. C.U. circuit defective.	Check C.U. circuit output at pin A5-2 with an oscilloscope. If signal is steady (not changing or erratic), circuit is functioning correctly.
	Note: Connect the oscilloscope external sync input to pin A50P36-12 for all waveform measurements. All waveform parameters appear on applicable block diagrams in Chapter 4.		
		c. C.U. circuit output erratic.	Disconnect N-Timing gate input from ratio and control circuit. If C.U. circuit starts to function correctly, that is, begins divide by ten in a non-erratic fashion, replace ratio and control circuit A36 (paragraph 44 b). If readout indication still erratic or malfunctioning, replace C.U. circuit A5 (paragraph 44 b).
15.	Erratic measurements. Repeated measurement error indication on mid and high bands.	a. Input sampler circuits.	Connect an oscilloscope to test point 3 on the ratio gate circuit (A29) and observe waveform. If waveform is present and constant, I.C., S.C., F.S., I.S., and ratio gate circuits are functioning correctly.

* Measurement Error Indication: Readout display continuously resets to zero's or the preset number.

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable trouble	Checks and Corrective Measures
15. (cont.)		b. I.C. Circuit defective.	Connect an oscilloscope to test point located on rear end of I.C. circuit and observe waveform. If waveform is present and constant, I.C. circuit is functioning correctly. If waveform is absent or shifting, replace I.C. circuit A3 (paragraph 44b).
		c. S.C. circuit defective. I.C. circuit functioning correctly.	Connect an oscilloscope to S.C. circuit rear connector and observe output waveform. If waveform is present and constant with a frequency between 9 and 10 MHz, S.C. circuit is functioning correctly. If waveform is absent or shifting, replace S.C. circuit A4 (paragraph 44 b).
		d. F.S. circuit defective.	Connect an oscilloscope to pin A50P1-17 and observe waveform. Frequency is 1.5 ±0.1 KHz. Connect the oscilloscope to F.S. circuit output cable and observe waveform. If waveforms are present for each check, the circuit is functioning correctly. (This waveform may shift and still be functioning correctly.) If waveforms are absent or out-of-tolerance, replace F.S. circuit A1-A24 (paragraph 44 b).
		e. I.S. circuit (or power divider defective).	Connect an oscilloscope to pin A50P31-6 and observe the I.S. circuit output waveform. It waveform is present and continuous, the I.S. circuit is functioning correctly. If waveform is weak or absent, perform a continuity check of power divider input and output cable assemblies and cable connectors. If waveform remains weak or absent after the continuity check, replace

ORIGINAL

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable trouble	Checks and Corrective Measures
15. (cont.)			I.S. circuit A31 (paragraph 44 b). If after performing the above check satisfactory results are not obtained, replace power divider A48Z1.
16.	Input sampler circuits functioning correctly at ratio gate test point 3 although measurement errors continue to occur.	a. Ratio gate or A logic circuits defective.	a. Connect the oscilloscope external sync to pin A50P29-13 and observe the ratio gate pulse input to the ratio gate circuit. Observe that the ratio gate pulse is a division-by-2 or a division-by-8 of the f_2 (1.5KHz) frequency.
	Note: All checks of the ratio gate circuit, A logic circuit, B logic circuit, and the display timer in the reset circuit, should be synchronized to the ratio gate pulse at pin A50P29-13.		
			b. If the ratio gate pulse is present at pin A50P30-13, check the ratio gate circuit output at pin A50P29-17. The ratio gate output will present groups of pulses with a repetition rate that will be the same as observed at pin A50P29-13. If input is absent, check and replace A logic circuit A25 (paragraph 44 b). If waveform at A50P29-17 is absent, replace the ratio gate circuit A29 (paragraph 44 b).
17.	Measurement error indication fail to occur when error exists.	a. B logic circuit defective.	a. Connect an oscilloscope to pin A50P27-6 and observe waveform . If waveform is absent, repeat step 15 c. and d.

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable trouble	Checks and Corrective Measures
17. (cont.)			b. If waveform is present, (groups of pulses as in step 16 b), check B logic circuit outputs at pins A50P26-13 and A50P27-11.
			c. If single burst-of-N pulses are present, circuit is functioning correctly. If waveform pulses are absent, replace B logic circuit A27 (paragraph 44 b.).
			d. If waveform is present at A50P27-11 (the single burst-of-N pulses) circuit is functioning correctly. If waveform is absent at A50P27-13 odd even F/F is defective, replace B logic circuit A27 (paragraph 44 b.).
		b. Parity logic circuit defective. (1), absence of single burst-of-N pulse.	Connect an oscilloscope to pin A50P26-16 and observe waveform. If waveform is present and varies only when input frequency to frequency counter is varied, parity logic circuit is functioning correctly. If waveform varies, replace parity logic circuit A26 (paragraph 44 b). If waveform is absent, check waveform present at pin A50P26-13. If waveform is present at A50P26-13 replace parity logic circuit A26. If waveform is absent, check for alternate reset pulses at pin A50P26-14. If waveform is present, replace parity logic circuit A26; if waveform is absent, repeat step 17 a.

ORIGINAL

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable trouble	Checks and Corrective Measures
17. (cont.)		(2) Absence of error reset pulse.	Connect the oscilloscope to pin A50P26-4 and observe waveform. If waveform is present only when the input frequency to the display indicator is varied, the parity logic circuit is functioning correctly. If waveform is present regardless of the adjustment to the input frequency, replace the parity logic circuit A26.
		(3) Absence of A reset pulse.	Connect an oscilloscope to pin A50P26-6 and observe waveform. If waveform is present, A reset pulse circuit is functioning correctly. If waveform is absent, replace parity logic circuit A26.
		(4) Absence of greater-than eight pulse.	Connect an oscilloscope to pin A50P26-11 and observe waveform. If waveform is present, parity logic, ratio and control and 2.5 MHz DCU (A38) are functioning correctly. If waveform is absent, check for waveform at pin A50-P36-11. If waveform is present, replace 2.5 MHz DCU (A38). If waveform is present in step 17 b. (1), replace ratio and control circuit (A36).
		c. 1-MHz oscillator defective. The EXT/INT oscillator switch should always be considered with this problem.	a. Connect an oscilloscope to pin A50P36-17 and observe waveform. If waveform is present, 1-Mc oscillator is functioning correctly. If waveform is absent, repair or replace 1-MHz oscillator A47Y1.

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable trouble	Checks and Corrective Measures
17. (cont.)			b. Connect an oscilloscope to pin A50P36-14 and observe waveform. If waveform is present, 1-MHz wave-shaping circuit is functioning correctly. If waveform is absent, replace ratio and control circuit A36.
		d. Time-Base generator circuit defective.	a. Connect an oscilloscope to pin A50P36-15 and observe 1-KHz pulses. If pulses are present, 2.5 MHz DCUs (A42, A43, A44) are functioning correctly. If waveform is absent, proceed to step b.
			b. Connect an oscilloscope to pin A50P44-7 and observe 10-KHz pulses. If waveform is present, replace 2.5 MHz DCU A44 (paragraph 44 b.).
			c. Connect an oscilloscope to pin A50-P43-7 and observe 100-KHz pulses. If waveform is present, replace 2.5 MHz DCU A43 (paragraph 44 b). If waveform is absent, proceed to step d.

Note: 1. The term DCU is used to denote a decade counting unit.
2. Time base troubleshooting is for 7 digit instrument. A similar procedure should be followed for nine digit instruments.

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable trouble	Checks and Corrective Measures
17. (cont.)			d. Connect an oscilloscope to pin A50-P42-7 and observe 1-MHz pulses. If pulses are present, replace 2.5 MHz DCU A42 (paragraph 44 b.). If waveform is absent, proceed to step e. e. Connect an oscilloscope to pin A50-P37-17 and observe 1-MHz pulses. If pulses are present, replace time base delay A37. If waveform is absent, repeat 1-MHz oscillator check. f. Connect an oscilloscope to pin A50-P44-6 and observe 10 Hz pulses. If waveform is present, 2.5 MHz DCUs A43 and A44 are functioning correctly. If waveform is absent, proceed to step g. g. Connect an oscilloscope to pin A50-P46-7 and observe 100 Hz pulses. If waveform is present, replace 2.5 MHz DCU A44. If pulses are absent, proceed to step h. h. Connect an oscilloscope to pin A50-P45-7 and observe 1-KHz pulses mixed with 1-MHz pulses. If waveform is absent and steps a. and d. checks are satisfactory, proceed to step i.

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable trouble	Checks and Corrective Measures
17. (cont.)			i. Connect an oscilloscope to pin A50-P36-12 and observe the reset pulse. If reset pulse is absent, perform a checkout of the reset circuit. If the reset pulse is present, connect the oscilloscope to A50P36-10 and observe waveform. If both waveforms are present but step h. fails, replace the ratio and control circuit A37 (paragraph 46 b). If waveform at A50P36-10 is absent perform ratio DCUs A38 and A39 checkout procedure.
		e. Ratio DCUs defective.	a. Connect an oscilloscope to pin A50-P39-7 and observe waveform. If waveform is present, but is not present at A50P37-10 in step i, replace 250 KHz DCU A39 (paragraph 46 b). If waveform is absent, proceed to step b.
			b. Connect an oscilloscope to pin A50-P38-7 and observe waveform. If waveform is present, replace 2.5 MHz DCU A38 (paragraph 49 b). If waveform is absent, replace the ratio and control circuit A36.
			c. Repeat the greater-than-eight pulse check for the parity logic circuit.
		f. Ratio and control circuit start-stop multivibrator defective.	a. Connect an oscilloscope at N-Timing gate pulse test point 1 (A36TP1) and observe waveform. Vary the input frequency applied to the frequency counter and observe that waveform pulse-width will change. If the

ORIGINAL

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable trouble	Checks and Corrective Measures
17. (cont.)			waveform is absent, check the pulse input at pin A50P36-2 and A50P36-12. b. Connect an oscilloscope to pin A50-P36-2 and observe waveform. If waveform is present and time interval between pulses changes as the input frequency is varied, DCUs A42, A43, A44, A45 and A46 are functioning correctly and providing nine-carry pulse outputs; proceed to step d. If waveform is absent, proceed to step c. c. If waveform is absent in step b., but time base generator circuit check is satisfactory, successively remove DCUs A41 through A44 (in the reverse order) until the nine-carry pulse occurs. Printed circuit boards are removed and replaced with the instrument de-energized. If after removing a DCU the nine-carry pulse returns, replace the defective DCU with a new one. Adjust the oscilloscope sweep rate to display two nine-carry pulses. Observe as a DCU is replaced in the time-base generator circuit. The time interval between pulses increases. (As DCUs are removed the time interval between pulses will decrease). Replace any defective DCU.

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable Trouble	Checks and Corrective Measures
17. (cont.)			d. Connect an oscilloscope to pin A50-P36-12 and observe reset pulse. If the reset pulse and the nine-carry pulses are present, but the N-Timing pulse is absent in step a, replace the ratio and control circuit A36.
		g. Reset circuit defective.	a. Connect an oscilloscope to pin A50-P35-14 and observe the positive reset pulse. Connect the oscilloscope to pin A50P35-12 and observe the negative reset pulse. If either pulse is absent, replace the reset circuit A36 (paragraph 44b.).
			b. Connect the oscilloscope to pin A50-P35-11 and observe the read pulse waveform. If the read pulse is present, the reset circuit display timer is functioning correctly. If the read pulse is absent, connect the oscilloscope to pin A50P35-4 and observe the stop flip-flop pulse. If the stop flip-flop pulse is absent, replace the ratio and control circuit A36. If the pulse is present, perform step c.
			c. Connect an oscilloscope to pin A50-P35-16 and observe the f_2 sync waveform. If the pulse is present and the pulse requirements of step b are present, replace the reset circuit A35. If the f_2 sync pulse is absent, perform the F.S. circuit check step 15.

ORIGINAL

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable trouble	Checks and Corrective Measures
17. (cont.)		h. N-Ratio function defective.	Connect an oscilloscope to pin A50P32-2. Disconnect the RF input to the frequency counter. Adjust the oscilloscope controls for a slow-sweep-scan and observe the display (N-Ratio pulse) varies as a sawtooth voltage. If the waveform is present, the N-Ratio function circuits are functioning correctly. AD circuitry troubles can be positively identified by placing instrument in the manual trigger mode of operation. If instrument operates normally in the manual position trouble is in the AD circuits. If the waveform is absent, perform the A.D. circuit checkout procedure.
		(1) A.D. circuit defective.	a. Connect an oscilloscope to pin A50-P34-13. Vary the RF input frequency to the frequency counter and observe that the oscilloscope display will present a series of pulses. If the pulses are present while the RF input is being varied, and are absent after the RF adjusting is stopped, the A.D. circuit is functioning correctly. If the pulses are present although the RF input is not being varied, proceed to step b. b. Connect an oscilloscope to pin A50-P34-17. Disconnect the RF input to the frequency counter. (Make sure the oscilloscope sweep is synchronized to the reset pulse.) Observe that the oscilloscope displays the error reset pulse waveform. If the

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable trouble	Checks and Corrective Measures
17. (cont.)			error reset pulse is absent, repeat the parity logic circuit A26 check-out procedure, If the waveforms are present, proceed to step c.
			c. Connect theoscilloscope input to A50P35-4 and observe the display pulse waveform. If waveform is absent, repeat ratio and control circuit A36 start-stop multivi-brator checkout procedure. If waveform is present, observe the error reset pulses and the display pulse. If waveforms are present, and no output pulse is generated in step a, replace the A.D. circuit A34.
		(2) Ramp generator circuit defective.	Connect an oscilloscope to pin A50P29-2 and disconnect the RF input to the freq-uency counter. Adjust the oscilloscope for a slow-sweep-scan and observe that the oscilloscope display (N-Ratio pulse) varies as a saw-tooth voltage. If the voltage fails to vary as a saw-tooth (or has steps in the waveform), success-ively connect the oscilloscope to pins 10, 11, 13, 14, 15, 16, and 17 of A50-P32 and observe that a binary division waveforms occur. If all the waveforms are present, replace the ramp gener-ator circuit A32, (paragraph 44 b). If a step in the saw-tooth waveform occurs or a binary division does not occur at pins 10, 11, 13 or 14 of A50P32, perform the divide-by-16 A33 checkout procedure. If a binary division does not occur at pins

ORIGINAL

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable trouble	Checks and Corrective Measures
17. (cont.)			15,16 or 17 of A50P32, perform the divide-by-8 circuit (A34) checkout procedure.
		(3) Divide-by-16 circuit defective.	Connect an oscilloscope to pin A50P33-6 and observe waveform. If pulses are present, while no binary division occurs at pins 10, 11, 13 and 14 of A50P32, replace the divide-by-16 circuit A33 (paragraph 44 b). If all the binary divisions occur, perform the divide-by-8 circuit (A34) checkout procedure.
		(4) Divide-by-8 circuit defective.	Connect an oscilloscope to pin A50P34-6 and observe waveform. If waveform is absent, replace the divide-by-16 circuit. If the waveform is present, successively connect the oscilloscope to pins 15, 16, or 17 of A50P32 and observe that a binary division waveform occurs. If all the waveforms are present, replace the ramp generator circuit A32. If a binary division does not occur at pins 15, 16 or 17 replace the divide-by-8 circuit A34 (paragraph 44 b).
18.	Readout display is in error of fails to index correctly.	a. Read pulse is defective.	Connect an oscilloscope to pin A50P10-18. Note that the direct store switch is in the store position. Vary the RF oscillator input and observe the read pulse waveform on the oscilloscope. If the read pulse is present, the display circuit read pulse circuit is functioning correctly. If the read pulse is absent, perform a checkout of the reset circuit A36.

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable trouble	Checks and Corrective Measures
18. (cont.)	Note: The counter checks (A5, A9, A11, A13, A15, A17 and A19) in the totalizing chain and the associated memory readout circuits (A6, A8, A10, A12, A14, A16 and A18) checkout procedures are similar. Each counter provides a division-by-10 of the frequency applied to its input. Preliminary circuit checks may be made by substituting the same part number board in a socket for a suspected board. For nine digit instruments additional DCU and memory readout circuits are used. The checkout procedure is the same as noted for the seven digit instruments.		
		b. Any one or more memory readout circuits are defective.	a. Connect an oscilloscope to A50-P18-8. Vary the input frequency and note the BCD input. If pulses are present, successively connect the oscilloscope input to pins 10, 12, and 14 of A50P18 and observe the BCD output from the counter as shown on the 250 KHz decade counting unit timing function diagram in Chapter 4. If waveform appears as shown in the figure, the counter is functioning correctly. Replace the memory readout circuit A18 (paragraph 44 c). Memory readouts A8, A10, A12, A14, and A16 are checked out in a similar manner at their respective sockets. If any timing function is incorrect, perform the decade counter checkout. Proceed to step c. to checkout memory readout circuit A6 and the matrix circuit A7.

ORIGINAL

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable trouble	Checks and Corrective Measures
18. (cont.)			b. Perform the same checkout of memory readout A6 as performed in step b. at A50P18. (Refer to matrix circuit A7 timing functions figure for BCD input waveforms). If waveforms appear as shown in the figure, the C.U. circuit and the matrix circuit are functioning correctly. Replace memory readout A6 (paragraph 44 e.). If any timing function is incorrect, perform the matrix circuit checkout procedure.
		c. Matrix circuit defective.	Perform the C.U. circuit checkout procedures in step 14. If the C.U. circuit is functioning correctly, successively connect an oscilloscope input to pins 16, 6, 7, 17, and 2 and observe the quinary output from the C.U. circuit. (Refer to matrix circuit A7 timing functions figure for quinary input waveforms.) If waveforms appear as shown in the figure, the C.U. circuit is functioning correctly. Replace matrix circuit A7 (paragraph 44 b). If the waveforms are abnormal or absent, replace the C.U. circuit (paragraph 44 b).
		d. Totalizer decade counter defective.	a. Connect an oscilloscope to pin A50-P19-7. Adjust the oscilloscope controls for 10 pulses presentation. Connect the second input to the oscilloscope to pin A50P19-5 and observe

Table 13. Troubleshooting Chart (Con't)

Step	Symptom	Probable trouble	Checks and Corrective Measures
18. (cont.)			a single output pulse waveform. (A division-by-10 occurs as shown on the associated timing function diagram in chapter 4.) If a division-by-10 occurs correctly, proceed to step b. If the division-by-10 fails to occur, replace the decade counting unit (paragraph 44 b.).
			b. Successively connect an oscilloscope to pins 9, 11, 13, and 15 of A50P19 and observe the BCD output from the counter as shown on 250 KHz decade counting unit timing function diagram in Chapter 4. If waveforms appear as shown in the figure, the counter is functioning correctly. If the divide-by-10 pulse is produced in step a, but the waveforms in step b are absent or incorrect, replace the decade counting unit.

Note: The three types of decade counting units are checked out in a similar manner as detailed above. When the NOT function output is used, pins 8, 10, 12, and 14 are used. If the nine-carry function is used, pin 6 provides the output pulse.

ORIGINAL

Chapter 6

REPAIRS AND CALIBRATION

Section I REPAIRS

42. GENERAL

This section contains instructions for servicing repairs and adjustments of the frequency counter.

43. PARTS REPLACEMENT TECHNIQUES

Most of the parts of the instrument are removable without any special procedures. The following precautions should be observed.

a. Use a pencil-type soldering iron with a 40-watt maximum capacity. Do not use a soldering gun; damaging voltage can be inducted in components.

b. When soldering transistor leads, solder quickly. Whenever wiring permits, use a heat sink (such as long-nose pliers) between the soldered joint and the transistor. Use approximately the same length and dress of transistor leads as used originally.

c. When installing a shielded wire, reconnect shield to same tie point that it was removed from. Dress all wires in the same manner as removed. Route all wires in the same route as removed. Dress the coaxial cables to fit.

44. PARTS REMOVAL AND REPLACEMENT PROCEDURES

The following steps provide part removal and replacement procedures for the instrument.

a. Internal Fuse Replacement. Replacement of internal fuses is accomplished in the following manner:

(1) Remove the top cover as detailed in cover removal procedure, paragraph 41.

(2) Remove the suspected fuse from fuse mounting board on power supply chassis.

(3) Using a multimeter set at the R X 1 resistance range, check for continuity across the fuse.

(4) Continuity greater than 5 ohms will indicate a faulty fuse and will require replacement.

b. Printed Circuit Board Replacement.

Caution: The printed circuit boards may have long pigtails on the solder side of the board. Care should be exercized when removing a board as damage to the adjacent board components may result. Printed circuit boards are never removed when the instrument is energized.

No printed circuit board puller is used to remove boards. Simply rock slowly and pull out from socket. Be extra careful with the input circuit boards. When removing the double boards (A1-A24 or A5-A28), pull the individual board out of the socket, tag cables and disconnect cables from the associated connector, then lift board clear of chassis. Refer to step c for memory readout circuit board removal procedure.

c. Memory readout Circuit Board Removal. The memory readout printed circuit boards requires additional care when removing from the chassis. Remove and replace the boards in the following manner:

(1) Tilt rear end of board (opposite end to where the indicator tube is mounted) first as it is being removed from socket.

(2) Move board toward the rear of the chassis to clear indicator board from readout housing assembly.

(3) Remove board clear of chassis.

(4) Replacement is the reverse of removal.

(5) Refer to paragraph 44 d for the indicator tube removal procedures.

d. Numerical Indicator Tube Removal and Replacement. To remove the indicators it is first necessary to remove the associated memory readout circuit board. After the boards are removed the glow-tube is pulled from the mounting socket on the board.

e. Front Panel Removal. The front panel is removed in the following manner.

(1) Remove instruments top and bottom covers as detailed in paragraph 41.

(2) Remove front panel control knobs, loosen set screws and pull off.

(3) Remove power switch. Loosen locknut from rear of front panel, remove dress nut.

(4) Remove Reset switch. Loosen locknut from rear of front panel, remove dress nut.

(5) Remove Input power divider. Remove locknut and washer from front panel.

(6) Remove Probe Power jack. Remove locknut and washer from rear of front panel. Probe Power jack comes out the front. Tag and disconnect power leads.

(7) Remove mounting screws holding front dress panel. Remove panel.

(8) Remove polaroid plexiglass window. If installed with Option I remove RFI screen.

g. Front Panel Replacement. The front panel is installed by reversing the procedure outlined in 44 e.

Note: To find the front side of the poloroid filter, place it over a shiney surface object. If the shiney surface is still noticeable, the filter is reversed. If the shiney surface is dimmed, this is the front-outer side.

h. Air Filter Removal and Replacement. The blower fan air filter is removed and replaced by removing the two mounting screws.

i. Blower Fan Removal and Replacement. The blower fan is removed in the following manner.

(1) Remove screws retaining the air filter.

(2) Remove the four mounting screws, retaining the fan assembly.

(3) Tag and disconnect wires to the fan.

(4) Lift fan up, then tilt toward front of the chassis and lift clear of chassis.

(5) Replacement is the reverse of removal.

j. Printed Circuit Board Socket Removal and Replacement. The printed circuit board sockets are removed in the following manner.

(1) Remove the top and bottom covers to the instrument as detailed in paragraph 41.

(2) Remove the printed circuit board in the socket to be removed.

(3) Remove the printed circuit boards in the adjacent sockets to prevent damage to the printed circuit boards circuit components.

(4) Tag and remove each wire to socket pins; clip any common buss line as required where the printed circuit board sockets are located several sockets in from the end of the common buss line end.

(5) Loosen the socket mounting hardware and remove the damage socket from the chassis.

Note: Several sockets have threaded spacers as mounting nuts. These will require replacement on the same socket after installation of the new socket.

(6) Replacement is the reverse of removal.

k. Removal of Parts from Printed Circuit Boards. The procedure for removal of lead-mounted parts from boards is as follows.

Caution: Excessive heat will damage printed circuit boards. Use a 40-watt soldering iron with a 1/8 inch tip at a temperature not greater than 550 degrees F. Do not apply soldering iron for more than five seconds to any one area. Protect heat-sensitive parts with a heat sink placed between the part and the solder point.

(1) Cut component lead near circuit board or solder weld.

(2) Apply desoldering iron to lead stub.

(3) Remove lead from printed circuit board in the opposite direction it was mounted in.

l. Removing Parts on Printed Circuit Boards. Replace parts on the assembly printed circuit board in accordance with the following procedure.

(1) Assure minimum clearance of 1/32 inch between part and printed circuit board.

(2) Allow minimum of 1/8 inch between lead bend and body of part.

(3) Adjust clearance between part and printed circuit board with a spacer.

(4) Crimp protruding part leads prior to soldering.

(5) Solder with small-diameter, 60/40 rosin-core solder.

(6) Apply minimum heat that allows free flow of solder.

m. Removal and Replacement of Power-Handling Semiconductor Devices. When replacing power transistors, or high-wattage voltage reference (Zener) diodes, proceed as follows:

(1) Tag and unsolder the leads from the base and emitter terminals of the power transistor or the cathode of the high-wattage reference diode.

(2) Remove attaching screws, insulating sleeves (if used), washers and locking washers, noting their order of assembly so that it may be duplicated when the new power transistor (diode) is installed.

(3) Remove the old power-handling device and any mica insulating washer from the heat sink or chassis. Discard the old power-handling device, but save the mica insulating washer for re-use if a new insulating washer is not supplied with the new power-handling device.

(4) Apply a thin coating of silicone heat sink compound, such as Dow Corning No. 340 to mating surfaces of the new power handling device, the mica insulating washer (if used), and the heat sink or chassis.

(5) Install the new power handling device, assembling it and its attaching and insulating hardware to the chassis or heat sink in the order noted during removal of the old device.

(6) Tighten attaching hardware securely and connect and solder leads to the correct terminals of the power handling device. Wipe excess heat sink compound from the edge of the newly-installed power-handling device.

45. GENERAL

This paragraph contains calibration procedures for the frequency counter power supply and time-base generator circuits. The accuracy of the instrument circuits is dependent upon the accuracy of the 1-Mc oscillator crystal. Any deviation from the oscillators nominal frequency will insert an error into all frequency measurements.

46. CALIBRATION PROCEDURES

Perform the calibration procedures adjustments using voltmeter with a 1 percent (or better) accuracy. If unable to obtain any required indication, perform the troubleshooting procedures for the malfunctioning circuit.

a. Power Supply Calibration.

(1) +12 Volts Dc Circuit Calibration. Connect the voltmeter (adjusted for +12 volts dc) between fuse A47F4 and chassis ground. Observe the voltmeter indication and adjust the power supply regulator +12 ADJ control (A47A1R4) for +12 ± 0.12 volts dc.

(2) -12 Volts Dc Circuit Calibration. Connect the voltmeter (adjusted for -12 volts dc) between fuse A47F3 and chassis ground. Observe voltmeter indication and adjust the power supply regulator -12 ADJ control (A47A1R3) for -12 ± 0.12 volts dc.

(3) +4.5 Volts Dc Circuit Calibration. Connect the voltmeter (adjusted for +4.5 volts dc) between fuse A47F2 and chassis ground. Observe the voltmeter indication and adjust the power supply regulator +4.5 ADJ control (A47A1R2) for +4.5 ±0.045 volts dc.

(4) -4.5 Volts Dc Circuit Calibration. Connect the voltmeter (adjusted for -4.5 volts dc) between fuse A47F1 and chassis ground. Observe the voltmeter indication and adjust the power supply regulator -4.5 ADJ control (A47A1R1) for -4.5 ±0.045 volts dc.

b. 1-Mc Oscillator Calibration. Perform the following procedure to calibrate the oscillator crystal.

(1) Set the EXT-INTERNAL switch to INTERNAL position.

(2) Connect the internal 1-Mc oscillator output at connector A49J1 to the oscilloscope vertical deflection input amplifiers.

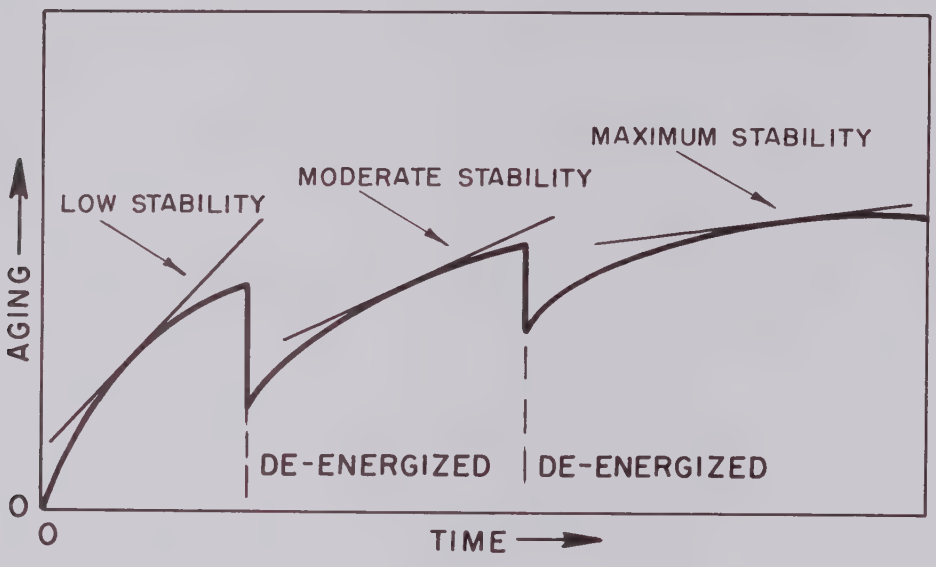
(3) Connect a 1 megahertz frequency standard * (10^{-9} accuracy) output to the oscilloscope horizontal deflection input amplifiers.

(4) Observe the lissajous pattern displayed on the oscilloscope screen.

(5) Slide the adjustment guard on the top of the 1-Mc oscillator to one side and adjust the oscillator trimmer control until the lissajous pattern stabilizes. If adjustment of the trimmer control fails to stabilize the lissajous pattern, replace the 1-Mc oscillator and repeat the calibration procedure.

* 10^{-10} with Option D.

Note: The aging rate of a crystal depends on the history of its environment. For fastest decrease in aging rate the oven should be energized at all times (instrument plugged into the power mains).



(6) Option D oscillators are adjusted by a course and fine frequency adjustments located on the side of the oven housing and with a single adjustment on the top of option B oscillators.

(7) When adjusting option D oscillators the lissajous pattern should be observed for a minute or more. The signal should be stable within one revolution in 100 seconds. Option B oscillators should remain stable within one revolution in ten seconds.

Note: The following adjustments are on the proprietary circuit boards and are included to enable qualified personnel to perform the more obvious alignment procedures. Due to the unique circuit design indiscriminate substitution of parts, or peaking of adjustments is inadvisable. If part replacement is necessary and controls do require adjusting caution should be the rule. Do not move in any way (other than absolutely necessary) the physical placement, space separation between coils (or wires) and in some instances lead length, of any component part or parts.

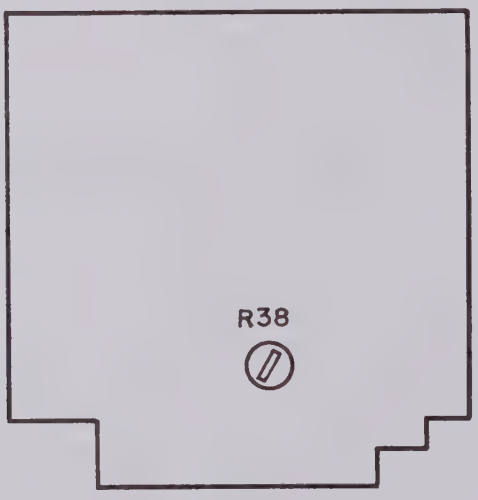
c. I.S. Circuit Adjustment. Replacement of the I.S. circuit board or of some component parts make adjustment of the amplitude control R38 necessary. This control is normally set at approximately 1/6 of a turn ccw from a maximum cw setting.

(1) Observe the waveform at A31-6 with a 6.5 GHz signal applied to the input jack.

(2) Reduce the input signal level to a minimum (0 dbm) signal level and adjust R38 for a maximum undistorted output at A31-6.

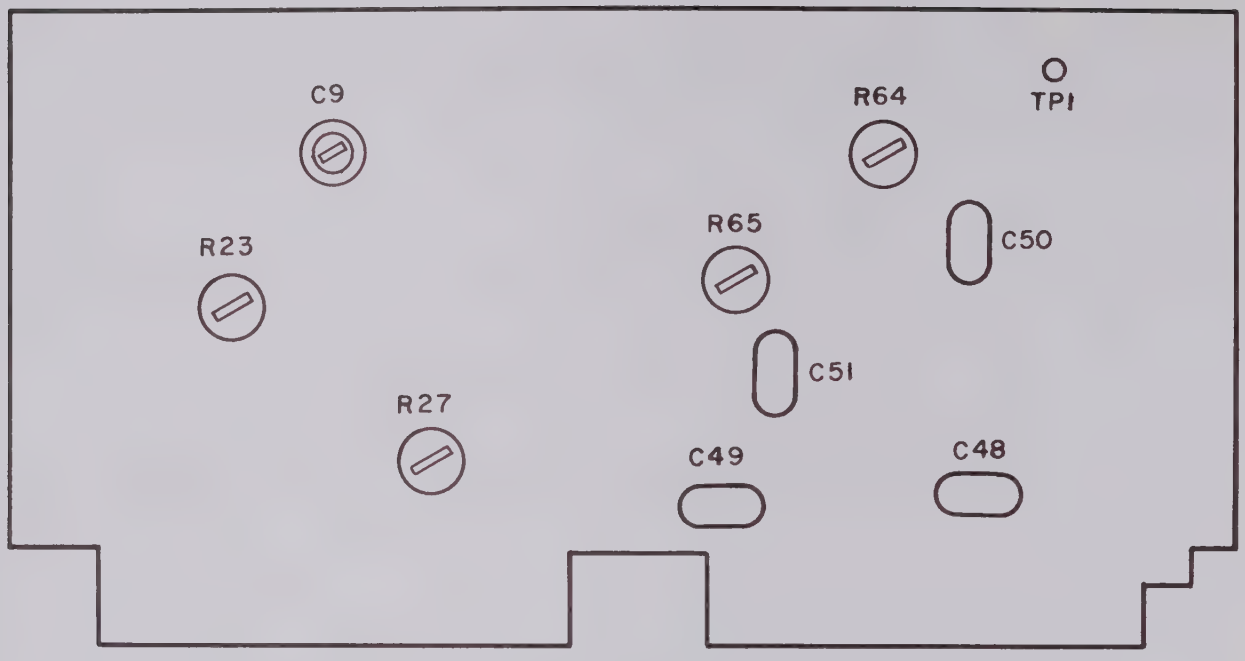
(3) Increase the input signal to an overload level (+ 7 dbm) and adjust R38 for an undistorted output at A31-6.

(4) Repeat steps (2) and (3) adjusting R38 for an optimum signal output at A31-6 with a 6.5 GHz input at minimum and maximum input levels.



d. F.S. Circuit Adjustments. Replacement of the F.S. circuit board or of some component parts within the circuitry may require adjustments. The F.S. circuit has five adjustment controls, some of which are inter-related and adjusting one effects the other. The adjustment procedure falls into two categories; 1) initial adjustment of the F.S. circuit; consists of, exciting the 1.5 KHz oscillator and adjusting for minimum 1.5 KHz modulation on the $f/n + f_2$ output signal, and 2) the re-adjusting of the $f/n + f_2$ signal for optimum instrument sensitivity at the high end of the measurement range.

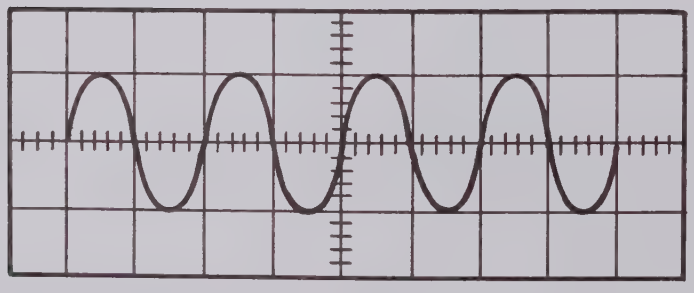
Initial adjustment requires removing the isolation shield on the board assembly.



(1) Initial Check and Adjustments.

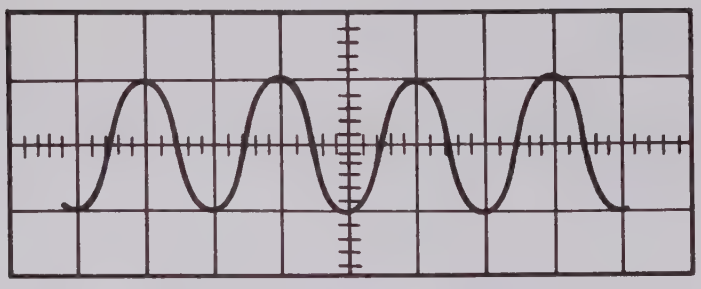
(a) Observe the 1.5 KHz oscillator at 24-17 and adjust R23 until a signal appears. Time separation between triggers should be approximately 666 microseconds (1.5 KHz). Observe the waveform at the base of Q3 and adjust R23 until the sinewave is slightly distorted. This requirement allows optimum operation at all temperature environments.

(b) 90° phase shift adjust. Observe the phase relationship between the 1.5 KHz 0° phase sinewave at the wiper of R64 (the junction between C48 and C50 is a convenient point) and the 1.5 KHz 90° phase shifted sinewave at the wiper of R65 (the junction between C49 and C51 is a convenient point). Adjust the scope to display two or three complete sinewaves using the 1.5 KHz signal at 24-17 as an external sync trigger.



0° phase at R64

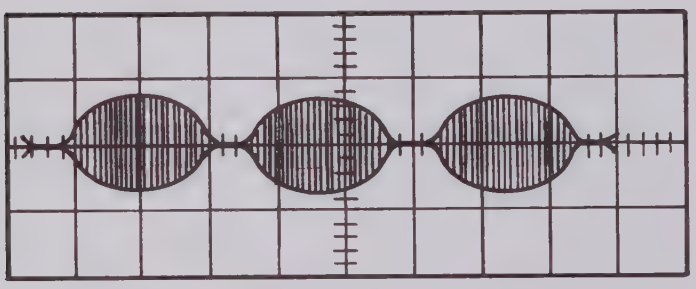
Adjust R27 for a 90° phase shift between the reference points of R64 and R65.



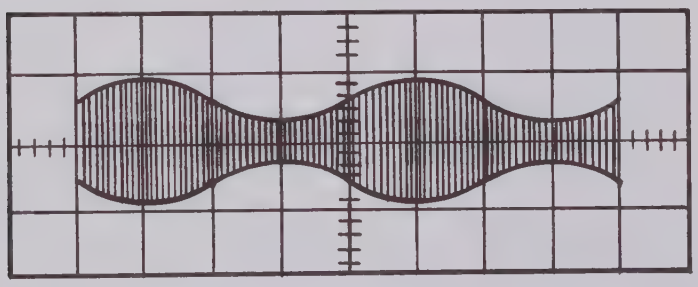
90°phase shifted at R65

Normally R27 will be rotated maximum cw for this desired phase shift. Trimmer capacitor C9 interacts with R27 for this adjustment and if the necessary phase shift is not possible by adjusting R27 alone rotate C9 slightly and then readjust R27.

(c) Minimum modulation envelope adjustment. Observe the RF waveform at TP1.



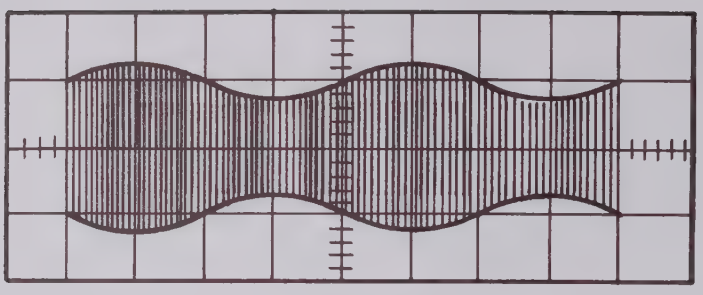
R27 and C9 not adjusted to provide a 90° phase shift.



Typical waveform with R27 and C9 set for 90° phase shift.

This signal is centered around 10 MHz with 1.5 KHz modulation. Using the 1.5 KHz signal at 24-17 for sync alternately adjust R64, R65 and C9 for minimum amplitude of the modulation envelope.

ORIGINAL



R64, R65 and C9 balanced for minimum modulation on signal.

NOTE: If R27 and C9 in (b) above are not properly adjusted for a 90° phase shift, step (c) will not reduce the ripple sufficiently for proper operation.

(2) Peaking the F.S. circuit for maximum sensitivity. The initial alignment procedure outlined above may require additional peaking after observing the counter in operation. At certain frequencies, usually the high end of the high band, the instrument will not read or error reset occurs. For optimum sensitivity readjustment of C9 (and to a lesser degree R64 and R65) is required.

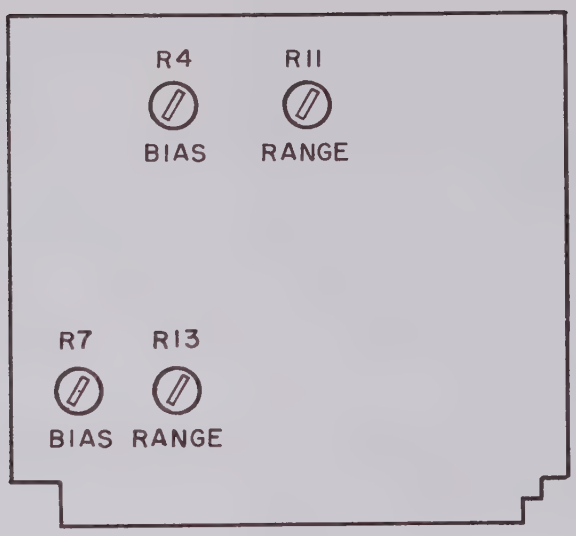
(a) Manipulate the trigger level control and the signal generator output until the counter reads the input frequency. Reduce the input level to just below this point. (Just after the instrument resets to zero's).

(b) Peak C9 (primarily), R64 and R65 to cause the counter to read the input frequency.

(c) Continue rocking the adjustments between reduced input signal level, changed trigger level and peaking C9 until the instrument reads all frequencies well within specifications. C9 normally has more influence on this adjustment although R64 and R65 need occasional peaking.

e. I.C. Circuit Adjustments. Replacement of the I.C. circuit board or of some component parts may require adjustment of the oscillator controls. The I.C. circuit is adjusted using the instrument frequency display as a meter. No other test equipment is required and adjustments are made with no input signal applied to the instruments. Two individual alignment steps are made relative to the Mid and High band frequency positions of the range switch. The adjustments are, the mid* frequency oscillator adjustment and the mid* frequency range adjustment; the high frequency oscillator adjustment and the high frequency range adjustment.

* Mid frequency oscillator adjustment is labeled Lo on the printed circuit board.



NOTE: No input signal.

(1) Mid Frequency Adjustments.

(a) Place range switch in the Mid band position.

(b) Place Test/Normal switch in the Test (T) position.

(c) Place Auto/Manual trigger switch to the Manual position and rotate manual trigger control full ccw.

(d) Observe frequency display and adjust R4 (TD bias) for an 8.75 MHz reading.

(e) Rotate manual trigger control full cw.

(f) Observe frequency displayed and adjust R11 (range control) for a 10.05 MHz reading.

(g) Repeat (d) and (f).

(2) High Frequency Adjustments.

(a) Place range switch in the High band position.

(b) Place Test/Normal switch in Test (T) position.

(c) Place Auto/Manual trigger switch to the Manual position and rotate the Manual trigger control to full ccw.

(d) Observe frequency displayed and adjust R7 (TD bias) for a 72 MHz reading.

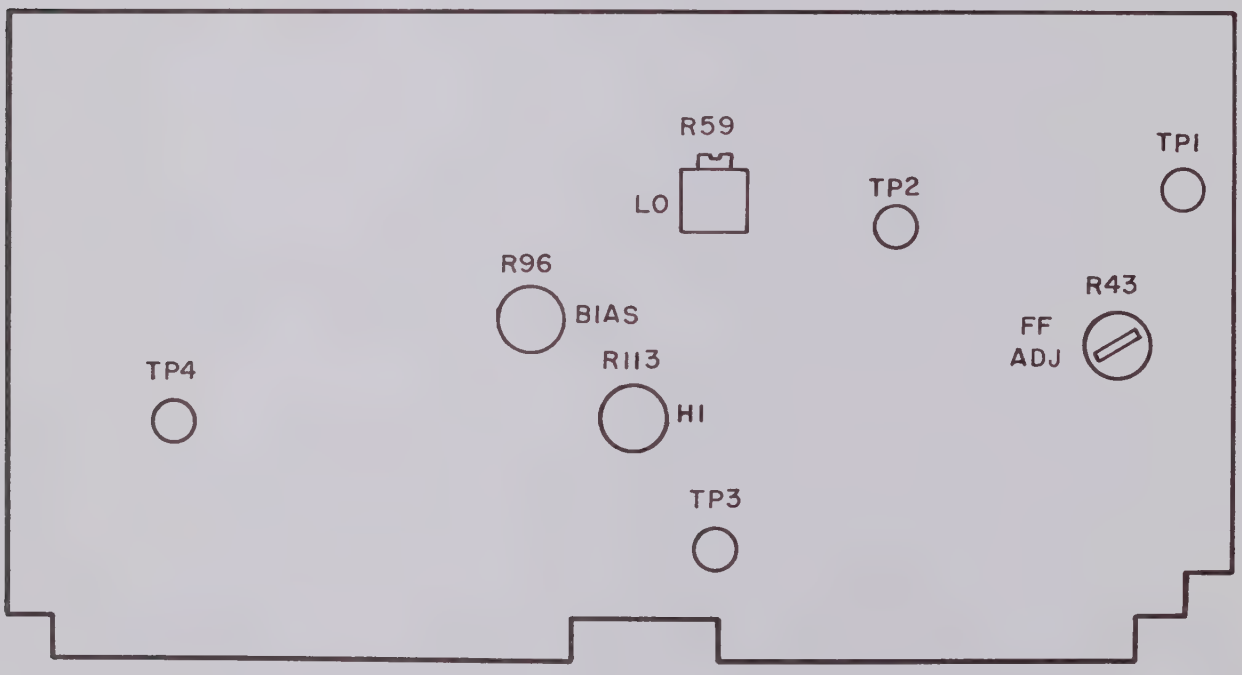
(e) Rotate Manual trigger control full cw.

(f) Observe frequency displayed and adjust R13 (range control) for an 82 MHz reading.

(g) Repeat (d) and (f).

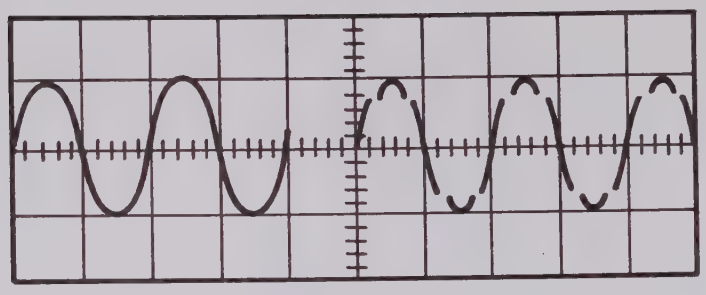
f. C.U. Circuit Adjustments. Replacement of the C.U. circuit board or of some component parts within the circuitry may make adjustments necessary. Normal operation of the board can be observed at TP1, TP3 and TP4. TP2 is used to monitor the binary operation as an intermediate troubleshooting check point. There are many matched components within the C.U. circuitry and if these are not in balance complete failure of the circuit will result. The following adjustment procedure is outlined showing waveforms and listing adjustments for circuit board replacement. This adjustment procedure will allow normal operation of the instrument in the environmental conditions under which the adjustment are made. A drastic change in temperature could cause internal circuit changes that may influence circuit operation. Eldorado checks all adjustments at -50°C, 25°C and 55°C.

The C.U. circuit can be divided into four functional blocks for adjustment procedure. These are the input wide band amplifier circuits, the binary circuits, the ring quinary circuits and the output amplifier circuit.



(1) Input wideband amplifier check and binary adjust.

(a) Observe waveform at TP1 with a 10 KHz signal applied to J2 and the N-Timing gate input J3 grounded. Adjust R43 for binary operation.



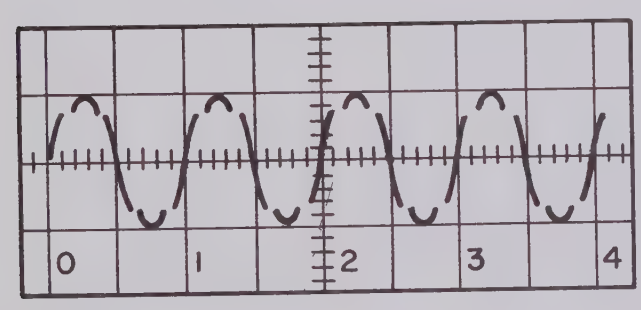
Binary inoperative Binary operating

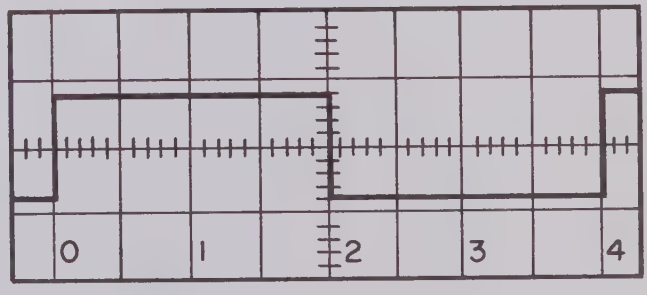
(b) Vary input frequency checking at 10 MHz, 40 MHz, 80 MHz and 130 MHz. TD binary should continue to count with input sensitivity of at least -20 dbm. Readjustment of R43 may be necessary to meet the -20 dbm sensitivity.

(2) Binary Count Check.

(a) Observe waveform at TP3 with a 10 KHz signal applied to J2 and the N-Timing gate J3 grounded.

(b) The output at TP3 should be a divided-by-two clean square wave replica of the input. Vary R43 in both directions and check for abnormal operation (does not divide-by-two etc.). Position R43 approximately in the center between points of abnormal operation.





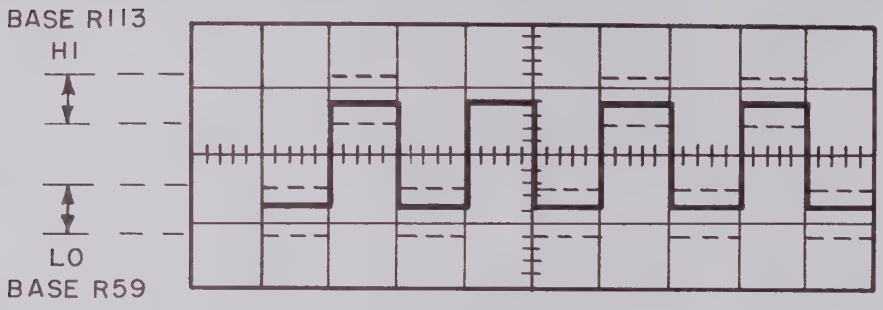
Normal Signal at TP1 Divide-by-Two Signal at TP3

(c) Repeat this procedure at 10 MHz, 40 MHz, 80 MHz, and 130 MHz positioning R43 at an optimum setting for all inputs. Output should be a clean stable square wave.

(3) Binary Output Level Adjust.

(a) Observe waveform at TP3 and vary the input frequency over the above mentioned range.

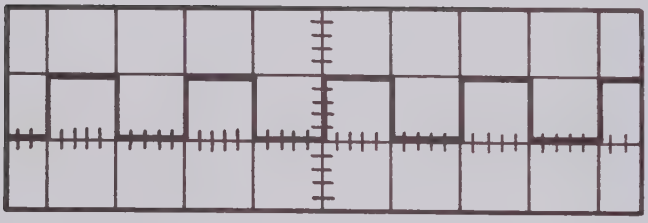
(b) Adjust R59 (Lo) and R113 (Hi) level controls for maximum amplitude of signal at TP3. An optimum setting should be established for all frequency inputs. R59 adjusts the low base level of the output and R113 adjusts the high base level.



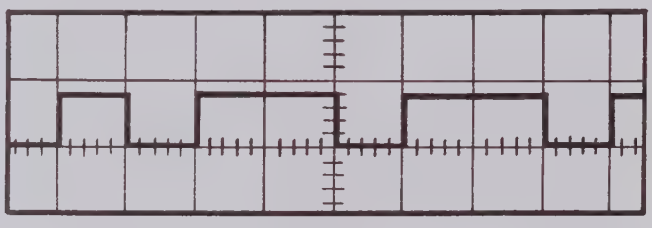
(4) Quinary ring counter bias adjust.

(a) Observe the waveform at TP4 with a 10 KHz signal applied to J2 and the N-Timing gate J3 grounded.

(b) The output should be a divide-by-ten count of the input. Adjust R96 in both directions until an abnormal count is received. Position R96 approximately in the center between the two extremes.



Normal Count



Abnormal Count

(c) Increase the frequency input to J2 and repeat step (b) at 10 MHz, 40 MHz, 80 MHz and 130 MHz. R96 should be positioned at the optimum setting to produce the desired divide-by-ten count down at all frequencies.

Chapter 7

IDENTIFICATION TABLE OF PARTS

Section I GENERAL

47. GENERAL

This section contains necessary information for ordering of replacement parts from either Eldorado Electronics or directly from commercial sources.

To use the parts list, first refer to the column on the left side of the page where the assembly of particular interest is referenced, then read down the page until the replacement part is located.

The quantities per item are listed in two columns. The first lists the total quantity per assembly, the second lists the total quantity per instrument. The Quantity Per Instrument column lists the totals for the 900 Series Counters. When two numbers appear in the column 7/9*; the first number (7) is the total for the seven digit counters Models 945/950, the second number (*9) is the total for the nine digit counters Models 946/951. This dual number breakdown of the 900 series counters is used only for PCB Assemblies. Electronic hardware is per assembly and per instrument.

48. ORDERING INFORMATION

To order replacement parts, address all orders or inquiries directly to:

CUSTOMER PARTS SERVICE DEPARTMENT
Eldorado Electronics
601 Chalomar Road
Concord, California (94520)

When ordering, specify the following information for each part:

a. Model and complete serial number.

b. Complete part description including: the assembly designation, part designation and part number.

49. CODE LIST OF MANUFACTURERS

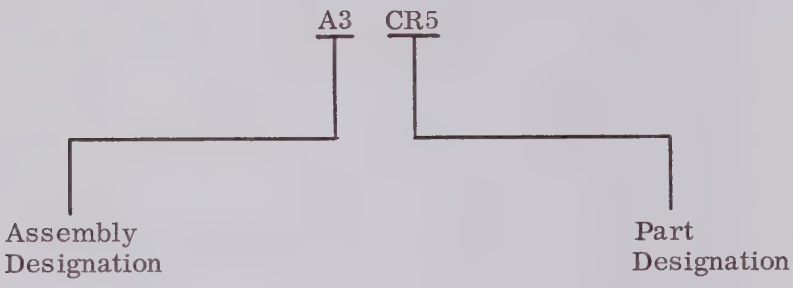
Coded manufacturer designations referenced throughout the parts list are further expanded in this section so that spare or replacement parts may be obtained directly with their respective manufacturers or vendors.

CODE	MANUFACTURER
AB	Allen Bradley Co., Milwaukee, Wisconsin
AD-YU	AD-YU Electronics Labs, Inc., Acton, Mass.
AML	Amphenol Electronics Corp., Chicago, Illinois
ARC	ARCO Electronics Inc., Great Neck LI, New York
BEN	Bendix Corp., Sidney, New York
BLD	Belden, Chicago, Illinois
BIR	Birnbach, New York, New York
BLY	Bliley Electric Co., Erie, Pennsylvania
BRNS	Bourns, Riverside, California
BUR	Burroughs Corp., Philadelphia, Pennsylvania
CAM	Cambridge Thermionic Corp., Cambridge, Mass.
CAN	Cannon Electric, Los Angeles, California
CAR	Carling Electric Inc., W. Hartford, Conn.
CRL	Centralab, Milwaukee, Wisconsin
CTS	Chicago Telephone Supply, Elkhart, Indiana
CIJ	Cinch-Jones, Chicago, Illinois
CML	Commercial Vendor
COR	Cornish Wire, New York, New York
CDC	Continental Device Corp., Hawthorne, Calif.
CH	Cutler-Hammer, Milwaukee, Wisconsin
CDE	Cornell-Dubilier Electric, Newark New Jersey
CW	Continental Wirt, Philadelphia, Pa.
DAL	Dale Products, Columbus, Nebraska
DEC	Delevan Electronics Corp., E. Aurora, N.Y.
DEL	Delco Radio Div., Kokomo, Indiana
DIA	Dialight Corp., Brooklyn, New York
ELC	ELCO Corp., Philadelphia, Pennsylvania
EE	Eldorado Electronics, Concord, California
EPC	Electron Products Co., Pasadena, California
ELM	Elmenco (ARCO), Los Angeles, California
ERR	Erie Resistor Corp., Erie, Pennsylvania
FAI	Fairchild Semiconductor, Mountain View, Calif.
FER	Ferroxcube Corp., Saugerties, New York
GE	General Electric Co., Auburn,New York
GI	General Instrument Corp., Newark, N.J.
GR	General Radio, West Concord, Massachusetts
GUL	Gulton Industries, Inc., Metuchen, New Jersey
HET	Hetherington, Sharon Hill, Pennsylvania
HOW	Howard Industries, Inc., Racine, Wisconsin
HPM	Honeywell Precision Meters, Manchester, N.H.
IER	IERC, Burbank, California
IMC	IMC Magnetics Corp., Westbury LI, New York
IDC	International Diode Corp., Jersey City, N. J.
JFD	J. F. D. Electronics Corp., Brooklyn, N.Y.
LIT	Littlefuse, Inc., Des Plaines, Illinois
MIL	Miller J.W., Los Angeles, California
MOT	Motorola, Phoenix, Arizona
OVN	Ovenaire, Inc., Charlottesville, Virginia
PEM	Penn. Eng. & Mfg. Corp., Doylestown, Penn.
PLC	Philco, Lansdale, Pennsylvania
RAY	Raytheon, Waltham, Massachusetts
ROT	Rotron, Hasbrouck, Louisiana
ROB	Robinson Co., The, Hawthorne, California
SAN	Sangamo Electric Co., Springfield, Illinois
SEA	Sealectro, Mamaroneck, New York
SEM	Semtech, Newbury Park, California
SIE	Siemens-und Halskeag, Munchen, Germany
SKF	SKF Industries, Inc., Philadelphia, Pennsylvania
SLO	Sloan, Sun Valley, California
SMH	Smith, H. H., Brooklyn, New York
SOL	Solitron Devices Inc., Norwood, New Jersey
SPR	Sprague Electric Co., Los Angeles, California
TI	Texas Instrument Inc., Dallas, Texas
THM	Thermolly, Dallas, Texas
TRS	Transitron Electric Corp., Wakefield, Mass.
TRI	Triad Transformer Corp., Venice, California
USCC	U. S. Capacitor Corp., Los Angeles, California
USE	U. S. Engineering Co., Inc., Van Nuys, Calif.
USMC	United Shoe Machinery Corp., Shelton, Conn.
VIK	Viking Industries, Canoga Park, California
VEM	Vemaline Products, Co., Franklin Lakes, New Jersey
WEI	Weinschel Engineering, Gaithersburg, Maryland
WSC	Wescap (SFE), San Fernando, California
WIL	Wilco, Indianapolis, Indiana

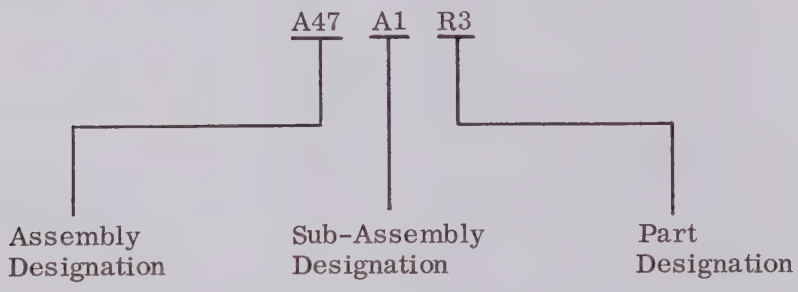
ORIGINAL

50. UNIT NUMBERING METHOD

The unit numbering method of assigning reference designations has been used to identify assemblies, sub-assemblies, and parts. An example of the unit numbering system is as follows:



Read from right to left as: Fifth diode (CR5) in the third assembly (A3).



Read from right to left as: Third resistor (R3) of first sub-assembly (A1) contained in forty seventh assembly (A47).

MEMORY READOUT CIRCUIT PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A6	Memory Readout PCB Assy.	EE	10-4000A		7/9*
A6CR1	Diode	EE	3-1001	1	69
A6CR2-3	Diode	EE	3-1005	2	2
A6I1	Nixie Indicator	BUR	B5092	1	7/9*
A6Q1-8	Transistor	EE	4-1002	8	56
A6Q9-18	Transistor	EE	4-1001	10	72
A6Q19	Transistor	CML	2N2712	1	8
A6R1, 6, 11, 14, 19, 22, 27, 30, 35	Resistor, Fixed Comp. 22K, 1/4W, 5%	AB	RC07GF223J	9	29
A6R2	Resistor, Fixed Comp. 47K, 1/4W, 5%	AB	RC07GF473J	1	14
A6R3	Resistor, Fixed Comp. 1K, 1/4W, 5%	AB	RC07GF102J	1	60
A6R4	Resistor, Fixed Comp. 150 ohm, 1/4W, 5%	AB	RC07GF151J	1	10
A6R5	Not Used				
A6R7, 12, 15, 20, 23, 31, 36, 50	Resistor, Fixed Comp. 33K, 1/4W, 5%	AB	RC07GF333J	8	100
A6R8-9	Resistor, Fixed Comp. 1.8K, 1/4W, 5%	AB	RC07GF182J	2	26
A6R10	Not Used				
A6R13, 18, 21, 26, 28, 34	Resistor, Fixed Comp. 6.8K, 1/4W, 5%	AB	RC07GF682J	6	65
A6R16, 17, 24, 25, 32, 33	Resistor, Fixed Comp. 2.7K, 1/4W, 5%	AB	RC07GF272J	6	60
A6R37	Resistor, Fixed Comp. 82K, 2W, 5%	AB	RC42GF823J	1	8
A6R38-45	Resistor, Fixed Comp. 27K, 1/4W, 5%	AB	RC07GF273J	8	62
A6R46	Resistor, Fixed Comp. 12K 1/4W, 5%	AB	RC07GF123J	1	18
A6XI1	Socket Tube	CIJ	SK128	1	7/9*

MATRIX CIRCUIT PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A7	Matrix PCB Assy.	EE	10-3933B	1	1
A7C1	Capacitor, Ceramic Disc .01uf, 50wvdc	SPR	TG-S10	1	19
A7C2-3	Capacitor, Plastic Film .1uf, 250wvdc	SIE	B32-234-S3104	2	52
A7CR1-5	Diode	TRS	S570G	5	8
A7Q1-17	Transistor	CML	2N404	17	29
A7R1, 3, 8, 11, 15, 20	Resistor, Fixed Comp.1.8K, 1/4W, 5%	AB	RC07GF182J	6	Ref.
A7R2, 6, 12,	Resistor, Fixed Comp. 22K, 1/4W, 5%	AB	RC07GF223J	3	Ref.
A7R4, 13, 21, 26	Resistor, Fixed Comp. 15K, 1/4W, 5%	AB	RC07GF153J	4	9
A7R5, 14	Resistor, Fixed Comp. 47K, 1/4W, 5%	AB	RC07GF473J	2	Ref.
A7R7, 9, 16, 19	Resistor, Fixed Comp. 1.5K, 1/4W, 5%	AB	RC07GF152J	4	16
A7R10	Resistor, Fixed Comp. 27K, 1/4W, 5%	AB	RC07GF273J	1	Ref.
A7R17	Resistor, Fixed Comp. 56 ohm, 1/4W, 5%	AB	RC07GF560J	1	1
A7R18, 22	Resistor, Fixed Comp. 1K, 1/4W, 5%	AB	RC07GF102J	2	Ref.
A7R23	Resistor, Fixed Comp. 82 ohm 1/4W, 5%	AB	RC07GF820J	1	1
A7R24	Resistor, Fixed Comp. 8.2K, 1/4W, 5%	AB	RC07GF822J	1	5
A7R25	Resistor, Fixed Comp. 5.6K, 1/4W, 5%	AB	RC07GF562J	1	13

25 MHZ DECADE COUNTING UNIT PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A9	25 MHz Decade Counting Unit PCB Assy.	EE	10-3968 A		1
A9C1, 2, 19, 20	Capacitor, Plastic Film .1 uf, 250 wvdc	SIE	B32-234-S3104	4	Ref.
A9C3, 4, 17	Capacitor, Dipped Mica 33 pf, 500 wvdc, 5%	SAN	D155F330J0	3	5
A9C5, 6	Capacitor, Dipped Mica 15 pf, 500 wvdc, 5%	SAN	D155F150J0	2	2
A9C7, 8, 11, 12, 15	Capacitor, Dipped Mica 27 pf, 500 wvdc, 5%	SAN	D155F270J0	5	9
A9C9, 10	Capacitor, Dipped Mica 22 pf, 500 wvdc, 5%	SAN	D155F220J0	2	6
A9C13, 14, 16, 18	Capacitor, Dipped Mica 39 pf, 500 wvdc, 5%	SAN	D155F390J0	4	22
A9CR1-32	Diode	CDC	CD6267	32	112
A9L1	Inductor, Ferrite Bead	FER	56-590-65/3B	1	
A9Q1-10	Transistor	MOT	MPS3640	10	19
A9R1, 7, 15, 23, 27, 36, 40, 45	Resistor, Fixed Comp. 68K, 1/4W, 5%	AB	RC07GF683J	8	28
A9R2, 8, 16, 17, 28, 29, 41, 46	Resistor, Fixed Comp. 10K, 1/4W, 5%	AB	RC07GF103J	8	58
A9R3, 11, 19, 22, 47	Resistor, Fixed Comp. 18K, 1/4W, 5%	AB	RC07GF183J	5	10
A9R4, 10	Resistor, Fixed Comp. 4.7K, 1/4W, 5%	AB	RC07GF472J	2	16
A9R5, 12	Resistor, Fixed Comp. 510 ohm, 1/4W, 5%	AB	RC07GF511J	2	2
A9R6, 13, 21, 26, 34, 39, 44, 50	Resistor, Fixed Comp. 270 ohm, 1/4W, 5%	AB	RC07GF271J	8	18
A9R9, 33, 38	Resistor, Fixed Comp. 820 ohm, 1/4W, 5%	AB	RC07GF821J	3	11
A9R14, 32, 51	Resistor, Fixed Comp. 1K, 1/4W, 5%	AB	RC07GF102J	3	Ref.

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A9R18, 24, 42, 48	Resistor, Fixed Comp. 5.6K, 1/4W, 5%	AB	RC07GF562J	4	Ref.
A9R20, 25, 43, 49	Resistor, Fixed Comp. 680 ohm, 1/4W, 5%	AB	RC07GF681J	4	8
A9R30, 37	Resistor, Fixed Comp. 6.8K, 1/4W, 5%	AB	RC07GF682J	2	Ref.
A9R31, 35	Resistor, Fixed Comp. 1.2K, 1/4W, 5%	AB	RC07GF122J	2	31

2.5 MHz DECADE COUNTING UNIT

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A11	2.5 MHz Decade Counting Unit PCB Assy.	EE	10-3967		2/9*
A11C1, 2, 19, 20	Capacitor, Plastic Film .1 uf, 250 wvdc	SIE	B32-234-S3104	4	Ref.
A11C3, 4	Capacitor, Dipped Mica 33 pf, 500 wvdc, 5%	SAN	D155F330J0	2	Ref.
A11C5, 6, 16, 17	Capacitor, Dipped Mica 27 pf, 500 wvdc, 5%	SAN	D155F270J0	4	Ref.
A11C7, 8, 15, 18	Capacitor, Dipped Mica 47 pf, 500 wvdc, 5%	SAN	D155F470J0	4	19
A11C9, 10, 13, 14	Capacitor, Dipped Mica 39 pf, 500 wvdc, 5%	SAN	D155F390J0	4	Ref.
A11C11-12	Capacitor, Dipped Mica 68 pf, 500 wvdc, 5%	SAN	D155F680J0	2	2
A11CR1-14	Diode	CDC	CD6267	14	Ref.
A11L1	Inductor, Ferrite Bead	FER	56-590-65/3B	1	2
A11Q1-8	Transistor	MOT	MPS3640	8	Ref.
A11Q9	Transistor	TI	2N3702/2N3638	1	22
A11R1, 7	Resistor, Fixed Comp. 1.8K, 1/4W, 5%	AB	RC07GF182J	2	Ref.
A11R2, 8, 14, 23, 28, 37, 42, 50	Resistor, Fixed Comp. 68K 1/4W, 5%	AB	RC07GF683J	8	Ref.
A11R3, 9, 15, 16, 29, 30, 43, 44, 46, 51, 55	Resistor, Fixed Comp. 10K, 1/4W, 5%	AB	RC07GF103J	11	Ref.
A11R4, 10, 56	Resistor, Fixed Comp. 6.8K, 1/4W, 5%	AB	RC07GF682J	3	9
A11R5	Resistor, Fixed Comp. 1.5K, 1/4W, 5%	AB	RC07GF152J	1	Ref.
A11R6, 12, 21, 27, 35, 41, 49, 54	Resistor, Fixed Comp. 100 ohm, 1/4W, 5%	AB	RC07GF101J	8	56
A11R11, 20, 26, 34, 40, 48, 53, 57	Resistor, Fixed Comp. 1K, 1/4W, 5%	AB	RC07GF102J	8	Ref.

2.5 MHz DECADE COUNTING UNIT PARTS LIST (Cont.)

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A11R13	Resistor, Fixed Comp. 2.7K, 1/4W, 5%	AB	RC07GF272J	1	Ref.
A11R17, 24, 31, 38, 47, 52	Resistor, Fixed Comp. 3.9K, 1/4W, 5%	AB	RC07GF392J	6	11
A11R18, 25, 32, 39	Resistor, Fixed Comp. 4.7K, 1/4W, 5%	AB	RC07GF472J	4	Ref.
A11R19, 22	Resistor, Fixed Comp. 3.3K, 1/4W, 5%	AB	RC07GF332J	2	44
A11R33, 36	Resistor, Fixed Comp. 5.6K, 1/4W, 5%	AB	RC07GF562J	2	Ref.
A11R45	Resistor, Fixed Comp. 39K, 1/4W, 5%	AB	RC07GF393J	1	8

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A13	250 KHz Decade Counting Unit PCB Assembly	EE	10-3966A		5/7*
A13C1, 2, 19, 20	Capacitor, Plastic Film .1 uf, 250 wvdc	SIE	B32-234-S3104	4	Ref.
A13C3, 4, 18	Capacitor, Dipped Mica 220 pf, 500 wvdc, 5%	SAN	D155F221J0	3	6
A13C5, 6, 16, 17	Capacitor, Dipped Mica 270 pf, 500 wvdc, 5%	SAN	D155F271J0	4	8
A13C7, 8, 15	Capacitor, Dipped Mica 470 pf, 500 wvdc, 5%	SAN	D155F471J0	3	10
A13C9, 10, 13, 14	Capacitor, Dipped Mica 390 pf, 500 wvdc, 5%	SAN	D155F391J0	4	Ref.
A13C11, 12	Capacitor, Dipped Mica 680 pf, 500 wvdc, 5%	SAN	D155F681J0	2	2
A13CR1-14	Diode	EE	3-1001	14	Ref.
A13L1	Inductor, Ferrite Bead	FER	56-590-65/3B	1	Ref.
A13Q1-8	Transistor	TI	2N3702(2N3638)	8	Ref.
A13R1, 5, 13	Resistor, Fixed Comp. 2.7K, 1/4W, 5%	AB	RC07GF272J	3	Ref.
A13R2, 11, 14, 22, 28, 36, 42, 50	Resistor, Fixed Comp. 68K, 1/4W, 5%	AB	RC07GF683J	8	Ref.
A13R3, 12	Resistor, Fixed Comp. 6.8K 1/4W, 5%	AB	RC07GF682J	2	Ref.
A13R4, 8	Resistor, Fixed Comp. 4.7K, 1/4W, 5%	AB	RC07GF472J	2	Ref.
A13R6	Resistor, Fixed Comp. 1.5K, 1/4W, 5%	AB	RC07GF152J	1	Ref.
A13R7, 10, 21, 25, 35, 40, 49, 54	Resistor, Fixed Comp. 100 ohm, 1/4W, 5%	AB	RC07GF101J	8	Ref.
A13R9, 20, 24, 34, 39, 48, 53	Resistor, Fixed Comp. 1K, 1/4W, 5%	AB	RC07GF102J	7	Ref.
A13R15, 16, 18, 27, 29, 30, 32, 41, 43, 44, 46, 51, 55	Resistor, Fixed Comp. 10K, 1/4W, 5%	AB	RC07GF103J	13	Ref.

250 KHz DECADE COUNTING UNIT PARTS LIST (Cont.)

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A13R17, 26	Resistor, Fixed Comp. 3.3K, 1/4W, 5%	AB	RC07GF332J	2	Ref.
A13R19, 23, 31, 37, 47, 52	Resistor, Fixed Comp. 3.9K, 1/4W, 5%	AB	RC07GF393J	6	Ref.
A13R33, 38	Resistor, Fixed Comp. 5.6K, 1/4W, 5%	AB	RC07GF562J	2	Ref.
A13R45	Resistor, Fixed Comp. 39K, 1/4W, 5%	AB	RC07GF393J	1	Ref.
A13R56	Resistor, Fixed Comp. 15K, 1/4W, 5%	AB	RC07GF153J	1	Ref.

OVERFLOW LOGIC PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A21	Overflow Logic PCB Assembly	EE	10-3999A		1
A21C1, 4	Capacitor, Dipped Mica 220 pf, 500 wvdc, 5%	SAN	D155F221J0	2	Ref.
A21C2, 3, 6, 7	Capacitor, Dipped Mica 270 pf, 500 wvdc, 5%	SAN	D155F271J0	4	Ref.
A21C5, 8	Capacitor, Dipped Mica 470 pf, 500 wvdc, 5%	SAN	D155F471J0	2	Ref.
A21C9, 10	Capacitor, Ceramic Disc .001 uf, 25 wvdc, 10%	CRL	DD102	2	3
A21C11, 12	Capacitor, Plastic Film .1 uf, 250 wvdc	SIE	B32-234-S3104	2	Ref.
A21CR1-4	Diode	EE	3-1001	4	Ref.
A21Q1-6, 8, 9	Transistor	CML	2N3702/2N3638	8	Ref.
A21Q7, 10	Transistor	EE	4-1001	2	Ref.
A21Q11	Transistor	CML	2N2712	1	Ref.
A21R1, 12, 14, 25	Resistor, Fixed Comp. 4.7K, 1/4W, 5%	AB	RC07GF472J	4	Ref.
A21R2, 13, 15, 26, 32, 42	Resistor, Fixed Comp. 33K, 1/4W, 5%	AB	RC07GF333J	6	Ref.
A21R3, 9, 16, 22	Resistor, Fixed Comp. 68K, 1/4W, 5%	AB	RC07GF683J	4	Ref.
A21R4, 10, 17, 23	Resistor, Fixed Comp. 3.9K, 1/4W, 5%	AB	RC07GF392J	4	Ref.
A21R5, 11, 18, 24, 49, 50	Resistor, Fixed Comp. 1K, 1/4W, 5%	AB	RC07GF102J	10	Ref.
A21R6, 8, 19, 21, 29, 33, 37, 44	Resistor, Fixed Comp. 6.8K, 1/4W, 5%	AB	RC07GF682J	8	Ref.
A21R7, 20	Resistor, Fixed Comp. 10K 1/4W, 5%	AB	RC07GF103J	2	Ref.
A21R28, 35, 36, 46	Resistor, Fixed Comp. 2.7K, 1/4W, 5%	AB	RC07GF273J	4	Ref.

OVERFLOW LOGIC PARTS LIST (Cont.)

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A21R30, 31, 39, 41, 48	Resistor, Fixed Comp. 22K, 1/4W, 5%	AB	RC07GF223J	5	Ref.
A21R34, 45	Resistor, Fixed Comp. 5.6K, 1/4W, 5%	AB	RC07GF562J	2	Ref.
A21R40	Resistor, Fixed Comp. 2.2K, 1/4W, 5%	AB	RC07GF222J	1	5
A21R43	Resistor, Fixed Comp. 100 ohm, 1/4W, 5%	AB	RC07GF101J	1	Ref.
A21R47	Resistor, Fixed Comp. 47K, 1/4W, 5%	AB	RC07GF473J	1	Ref.
A21R51-54	Resistor, Fixed Comp. 270 ohm, 1/4W, 5%	AB	RC07GF271J	4	Ref.

A LOGIC PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A25	A Logic PCB Assembly	EE	10-3414		1
A25C1, 2	Capacitor, Dipped Mica 180 pf, 100 wvdc, 5%	SAN	D151F181J0	2	3
A25C3, 4, 7, 8, 11, 12, 15, 16	Capacitor, Dipped Mica 39 pf, 100 wvdc, 5%	SAN	D151F390J0	8	16
A25C5, 6, 9, 10, 13, 14	Capacitor, Dipped Mica 47 pf, 100 wvdc, 5%	SAN	D151F470J0	6	14
A25C17, 18	Capacitor, Ceramic Disc .01 uf, 50 wvdc	SPR	TG-S10	2	Ref.
A25C19	Capacitor, Dipped Mica 270 pf, 100 wvdc, 5%	SAN	D151F271J0	1	Ref.
A25CR1-5, 7-13	Diode	CDC	CD6267	12	Ref.
A25CR6	Not Used				
A25CR14	Diode	TRS	S570G	1	8
A25Q1-8	Transistor	EE	4-1003	8	41
A25R1, 19, 28	Resistor, Fixed Comp. 100 ohm, 1/4W, 5%	AB	RC07GF101J	3	Ref.
A25R2, 3, 11, 12, 20, 21, 29, 30	Resistor, Fixed Comp. 220 ohm, 1/4W, 5%	AB	RC07GF221J	8	32
A25R4, 5, 37, 38	Resistor, Fixed Comp. 1K, 1/4W, 5%	AB	RC07GF102J	4	Ref.
A25R6, 7, 15, 16, 24, 25, 33, 34	Resistor, Fixed Comp. 3.3K, 1/4W, 5%	AB	RC07GF332J	8	Ref.
A25R8, 9, 17, 18, 26, 27, 35, 36	Resistor, Fixed Comp. 33K, 1/4W, 5%	AB	RC07GF333J	8	Ref.
A25R13, 14, 22, 23, 31, 32	Resistor, Fixed Comp. 1.2K, 1/4W, 5%	AB	RC07GF122J	6	Ref.

B LOGIC PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A27	B Logic PCB Assembly	EE	10-3415A		1
A27C1, 2, 5, 6, 9, 10, 13, 14	Capacitor, Dipped Mica 47 pf, 100 wvdc, 5%	SAN	D151F470J0	8	Ref.
A27C3, 4, 7, 8, 11, 12, 15, 16	Capacitor, Dipped Mica 39 pf, 100 wvdc, 5%	SAN	D151F390J0	8	Ref.
A27C17, 18	Capacitor, Ceramic Disc .01 uf, 50 wvdc	SPR	TG-S10	2	Ref.
A27C19	Capacitor, Dipped Mica 330 pf, 100 wvdc, 5%	SAN	D151F331J0	1	Ref.
A27CR1-5, 7-13	Diode	CDC	CD6267	12	Ref.
A27CR6	Not Used				
A27CR14	Diode	TRS	S570G	1	Ref.
A27Q1-8	Transistor	EE	4-1003	8	Ref.
A27R1, 10, 19, 28, 39	Resistor, Fixed Comp. 100 ohm, 1/4W, 5%	AB	RC07GF101J	5	Ref.
A27R2, 3, 11, 12, 20, 21, 29, 30	Resistor, Fixed Comp. 220 ohm, 1/4W, 5%	AB	RC07GF221J	8	Ref.
A27R4, 5, 38	Resistor, Fixed Comp. 1K, 1/4W, 5%	AB	RC07GF102J	3	Ref.
A27R6, 7, 15, 16, 24, 25, 33, 34	Resistor, Fixed Comp. 3.3K, 1/4W, 5%	AB	RC07GF332J	8	Ref.
A27R8, 9, 17, 18, 26, 27, 35, 36	Resistor, Fixed Comp. 33K, 1/4W, 5%	AB	RC07GF333J	8	Ref.
A27R13, 14, 22, 23, 31, 32	Resistor, Fixed Comp. 1.2K, 1/4W, 5%	AB	RC07GF122J	6	Ref.
A27R37	Resistor, Fixed Comp. 1.8K, 1/4W, 5%	AB	RC07GF182J	1	Ref.

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A26	P Logic PCB Assembly	EE	10-3978-C		1
A26C1, 10	Capacitor, Dipped Mica 1000 pf, 100 wvdc, 5%	SAN	D151F102J0	2	14
A26C2	Not Used				
A26C3, 6	Capacitor, Dipped Plastic .0047 uf, 75 wvdc, 20%	GUL	MIN-M-.0047M	2	4
A26C4, 5, 13	Capacitor, Dipped Plastic .0022 uf, 75 wvdc, 20%	GUL	MIN-M-.0022M	3	3
A26C7, 11, 12, 17, 19	Capacitor, Ceramic Disc .01 uf, 50 wvdc	SPR	TG-S10	5	Ref.
A26C8	Capacitor, Ceramic Disc. .001 uf, 1000 wvdc	CRL	DD102	1	Ref.
A26C9	Capacitor, Ceramic Disc. .22 uf, 25 wvdc, 20%	SPR	5C9	1	1
A26C14	Capacitor, Dipped Mica 470 pf, 500 wvdc, 5%	SAN	D155F471J0	1	Ref.
A26C15	Capacitor, Dipped Mica 330 pf, 500 wvdc, 5%	SAN	D155F331J0	1	3
A26C16, 18	Capacitor, Dipped Plastic .01 uf, 75 wvdc, 20%	GUL	MIN-M-.01M	2	3
A26C20-22	Capacitor, Plastic Film .1 uf, 250 wvdc	SIE	B32-234-S3104	3	Ref.
A26CR1, 8, 10, 11	Diode	CDC	CD6267	4	Ref.
A26CR2-7, 9, 12, 13	Diode	EE	3-1001	9	Ref.
A26Q1, 5, 6	Transistor	FAI	2N2924	3	3
A26Q2-4, 7	Transistor	CML	2N404	4	Ref.
A26Q8-11	Transistor	CML	2N708	4	7
A26R1	Resistor, Fixed Comp. 2.2K, 1/4W, 5%	AB	RC07GF222J	1	Ref.
A26R2, 26, 27, 35	Resistor, Fixed Comp. 3.3K, 1/4W, 5%	AB	RC07GF332J	4	Ref.
A26R3	Resistor, Fixed Comp. 10K, 1/4W, 5%	AB	RC07GF103J	1	Ref.

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A26R4	Resistor, Fixed Comp. 27K, 1/4W, 5%	AB	RC07GF273J	1	Ref.
A26R5	Resistor, Fixed Comp. 82K, 1/4W, 5%	AB	RC07GF823J	1	Ref.
A26R6, 15	Resistor, Fixed Comp. 47 ohm 1/4W, 5%	AB	RC07GF470J	2	8
A26R7, 17, 18	Resistor, Fixed Comp. 820 ohm 1/4W, 5%	AB	RC07GF821J	3	Ref.
A26R8	Resistor, Fixed Comp. 1.5K, 1/4W, 5%	AB	RC07GF152J	1	Ref.
A26R9, 41	Resistor, Fixed Comp. 6.8K, 1/4W, 5%	AB	RC07GF682J	2	Ref.
A26R10	Resistor, Fixed Comp. 3.9K, 1/4W, 5%	AB	RC07GF392J	1	Ref.
A26R11-12	Not Used				
A26R13	Resistor, Fixed Comp. 1.8K, 1/4W, 5%	AB	RC07GF182J	1	Ref.
A26R14	Resistor, Fixed Comp. 18K, 1/4W, 5%	AB	RC07GF183J	1	Ref.
A26R16	Resistor, Fixed Comp. 56K, 1/4W, 5%	AB	RC07GF563J	1	2
A26R19, 37,	Resistor, Fixed Comp. 27 ohm, 1/4W, 5%	AB	RC07GF270J	2	2
A26R20	Resistor, Fixed Comp. 390 ohm, 1/4W, 5%	AB	RC07GF391J	1	Ref.
A26R21	Resistor, Fixed Comp. 680 ohm, 1/4W, 5%	AB	RC07GF681J	1	Ref.
A26R22, 23	Resistor, Fixed Comp. 8.2K, 1/4W, 5%	AB	RC07GF822J	2	Ref.
A26R24	Resistor, Fixed Comp. 560K, 1/4W, 5%	AB	RC07GF564J	1	1
A26R25, 29, 33, 34	Resistor, Fixed Comp. 12K, 1/4W, 5%	AB	RC07GF123J	4	Ref.

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A26R28	Resistor, Fixed Comp. 15K, 1/4W, 5%	AB	RC07GF153J	1	Ref.
A26R30, 39	Resistor, Fixed Comp. 1.2K, 1/4W, 5%	AB	RC07GF122J	2	Ref.
A26R31, 32, 43	Resistor, Fixed Comp. 1K, 1/4W, 5%	AB	RC07GF102J	3	Ref.
A26R36	Resistor, Fixed Comp. 2.7K, 1/4W, 5%	AB	RC07GF272J	1	Ref.
A26R38	Resistor, Fixed Comp. 470 ohm, 1/4W, 5%	AB	RC07GF471J	1	9
A26R40	Resistor, Fixed Comp. 5.6K, 1/4W, 5%	AB	RC07GF562J	1	Ref.
A26R42	Resistor, Fixed Comp. 33 ohm, 1/4W, 5%	AB	RC07GF330J	1	2
A26TP1-3	Connector, Test Point	CAM	1597-2	3	6

R GENERATOR CIRCUIT PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A32	R Generator PCB Assembly	EE	10-3977C		1
A32C1	Not used				
A32C2	Capacitor, Solid Tantalum 56 uf, 15 wvdc, 10%	SPR	150D566X-9015R2	1	1
A32C3, 5	Capacitor, Plastic Film .33 uf, 250 wvdc	SIE	B32-232-S3334M	2	2
A32C4, 9	Capacitor, Ceramic Disc .005 uf, 50 wvdc.	SPR	TGD50	2	8
A32C6, 7	Capacitor, Dipped Mica 18 pf, 500 wvdc, 5%	SAN	D155F180J0	2	2
A32C8	Capacitor, Ceramic Disc. .01 uf	SPR	TG-S10	1	Ref.
A32L1-2	Inductor, 100 uh	DEC	1025-68	2	2
A32Q1-14	Transistor	CML	2N708	14	Ref.
A32R1	Not Used				
A32R2	Resistor, Fixed Comp. 750 ohm, 1/2W, 5%	AB	RC20GF751J	1	1
A32R3-6	Resistor, Metal Film 1.5K, 1/4W, 1%	IRC	MEA-TO	4	4
A32R7	Resistor, Metal Film 1.5K, 1/4W, 1/4%	IRC	MEA-TO	1	1
A32R8, 14	Resistor, Metal Film 750 ohm, 1/4W, 1/4%	IRC	MEA-TO	2	2
A32R9-13	Resistor, Metal Film 750 ohm, 1/4W, 1%	IRC	MEA-TO	5	5
A32R22, 24, 26, 28, 30, 32, 36-39, 34	Resistor, Fixed Comp. 100 ohm, 1/4W, 5%	AB	RC07GF101J	11	Ref.
A32R23, 25, 27, 29, 31	Resistor, Metal Film 1.82K, 1/4W, 1%	IRC	MEA-TO	5	5
A32R33, 35	Resistor, Metal Film 1.82K, 1/4W, 1/4%	IRC	MEA-TO	2	2

DIVIDE-BY-16 COUNTING UNIT PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A33	Divide-by-16 CU, PCB Assembly	EE	10-3412		1
A33C1, 2, 5, 6, 9, 10, 13, 14	Capacitor, Dipped Mica 47 pf, 500 wvdc, 5%	SAN	D155F470J0	8	Ref.
A33C3, 4, 7, 8, 11, 12, 15, 16	Capacitor, Dipped Mica 39 pf, 500 wvdc, 5%	SAN	D155F390J0	8	Ref.
A33C17, 18	Capacitor, Ceramic Disc .01 uf, 50 wvdc	SPR	TG-S10	2	Ref.
A33CR1-5, 7-13	Diode	CDC	CD6267	12	Ref.
A33CR6, 14, 15	Diode	TRS	S570G	3	Ref.
A33Q1-8	Transistor	EE	4-1003	8	Ref.
A33R1, 10, 19, 28	Resistor, Fixed Comp. 100 ohm, 1/4W, 5%	AB	RC07GF101J	4	Ref.
A33R2, 3, 11, 12, 20, 21, 29, 30	Resistor, Fixed Comp. 220 ohm, 1/4W, 5%	AB	RC07GF221J	8	Ref.
A33R4, 5	Resistor, Fixed Comp. 1K, 1/4W, 5%	AB	RC07GF102J	2	Ref.
A33R6, 7, 15, 16, 24, 25, 33, 34	Resistor, Fixed Comp. 3.3K, 1/4W, 5%	AB	RC07GF332J	8	Ref.
A33R8, 9, 17, 18, 26, 27, 35, 36	Resistor, Fixed Comp. 33K, 1/4W, 5%	AB	RC07GF333J	8	Ref.
A33R13, 14, 22, 23, 31, 32	Resistor, Fixed Comp. 1.2K, 1/4W, 5%	AB	RC07GF122J	6	Ref.

AD AND DIVIDE-BY-8 COUNTING UNIT PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A34	Divide-by-8 and AD Circuit PCB Assembly	EE	10-3992A		1
A34C1, 2, 5, 6, 9, 10	Capacitor, Dipped Mica 47 pf, 500 wvdc, 5%	SAN	D155F470J0	6	Ref.
A34C3, 4, 7 8, 11, 12	Capacitor, Dipped Mica 39 pf, 500 wvdc, 5%	SAN	D155F390J0	6	Ref.
A34C13, 14	Capacitor, Ceramic Disc .01 uf, 50 wvdc	SPR	TG-S10	2	Ref.
A34C15, 18	Capacitor, Dipped Mica 1000 pf, 100 wvdc, 5%	SAN	D151E102J0	2	Ref.
A34C16	Capacitor, Dipped Plastic .005 uf, 75 wvdc, 20%	GUL	MIN-M-.005M	1	1
A34C17	Capacitor, Dipped Mica 56 pf, 500 wvdc, 5%	SAN	D155F560J0	1	1
A34C19	Capacitor, Dipped Mica 470 pf, 500 wvdc, 5%	SAN	D155F471J0	1	Ref.
A34CR1-4, 6-10, 14	Diode	CDC	CD6267	10	Ref.
A34CR5	Diode	TRS	S570G	1	Ref.
A34CR11-13	Diode	CML	IN459	3	4
A34Q1-7, 10	Transistor	EE	4-1003	8	Ref.
A34Q8, 9	Transistor	CML	2N706A	2	7
A34R1-3	Resistor, Fixed Comp. 100 ohm, 1/4W, 5%	AB	RC07GF101J	3	Ref.
A34R4, 10, 12, 17, 20, 25	Resistor, Fixed Comp. 1.2K, 1/4W	AB	RC07GF122J	6	Ref.
A34R5, 9, 13, 18, 21, 26, 30	Resistor, Fixed Comp. 3.3K, 1/4W, 5%	AB	RC07GF332J	7	Ref.
A34R6, 11, 14, 19, 22, 27	Resistor, Fixed Comp. 33K 1/4W, 5%	AB	RC07GF333J	6	Ref.
A34R7, 8, 15, 16, 23, 24	Resistor, Fixed Comp. 220 ohm, 1/4W, 5%	AB	RC07GF221J	6	Ref.
A34R28	Resistor, Fixed Comp. 4.7K, 1/4W, 5%	AB	RC07GF472J	1	Ref.

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY	QTY. PER INST.
A34R29, 31, 33, 35	Resistor, Fixed Comp. 1K, 1/4W, 5%	AB	RC07GF102J	4	Ref.
A34R32, 36	Resistor, Fixed Comp. 10K, 1/4W, 5%	AB	RC07GF103J	2	Ref.
A34R34	Resistor, Fixed Comp. 2.2K, 1/4W, 5%	AB	RC07GF222J	1	Ref.
A34R37, 38	Resistor, Fixed Comp. 470 ohm, 1/4W, 5%	AB	RC07GF471J	2	Ref.

RESET CIRCUIT PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A35	Reset PCB Assy.	EE	10-3942C		1
A35C1, 10, 14, 16	Capacitor, Dipped Mica 1000 pf, 100 wvdc, 5%	SAN	D151F102J0	4	Ref.
A35C2	Capacitor, Dipped Plastic .01 uf, 75 wvdc	GUL	MIN-M-.01-M	1	Ref.
A35C3	Not used				
A35C4, 19-22	Capacitor, Plastic Film .1 uf, 250 wvdc	SIE	B32-234-S3104	5	Ref.
A35C5	Capacitor, Electrolytic 15 uf, 15 wvdc	SPR	TE1156	1	1
A35C6, 23	Capacitor, Ceramic Disc .005 uf, 50 wvdc	SPR	TG-D50	2	Ref.
A35C7, 8, 15	Capacitor, Ceramic Disc .01 uf, 50 wvdc	SPR	TG-S10	3	Ref.
A35C9	Capacitor, Dipped Mica 330 pf, 500 wvdc, 5%	SAN	D155F331J0	1	Ref.
A35C11, 18	Capacitor, Dipped Plastic .0047 uf, 75 wvdc	GUL	MIN-M-.0047-M	2	Ref.
A35C12, 17	Capacitor, Dipped Plastic .0022 uf, 75 wvdc	GUL	MIN-M-.0022-M	2	Ref.
A35C13	Capacitor, Electrolytic 2 uf, 15 wvdc	SPR	TE1149	1	1
A35CR1, 2, 4 6-10	Diode	EE	3-1001	8	Ref.
A35CR3	Diode, Zener	CDC	1N756A	1	1
A35CR5	Diode	CDC	1N459	1	Ref.
A35Q1-2, 4-6,	Transistor	CML	2N706A	5	Ref.
A35Q3	Transistor	CML	2N1671B	1	1
A35Q7, 8	Transistor	CML	2N404	2	Ref.
A35Q9	Transistor	CML	2N3053	1	1
A35R1, 3	Resistor, Fixed Comp. 8.2K, 1/4W, 5%	AB	RC07GF822J	2	Ref.
A35R2, 7, 12, 13, 40	Resistor, Fixed Comp. 10K, 1/4W, 5%	AB	RC07GF103J	5	Ref.

RESET CIRCUIT PARTS LIST (Cont.)

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A35R4, 16, 18, 21, 25, 29	Resistor, Fixed Comp. 100 ohm, 1/4W, 5%	AB	RC07GF101J	6	Ref.
A35R5, 6, 22, 31	Resistor, Fixed Comp. 1K, 1/4W, 5%	AB	RC07GF102J	4	Ref.
A35R8, 32	Resistor, Fixed Comp. 470 ohm, 1/4W, 5%	AB	RC07GF471J	2	Ref.
A35R9, 27	Resistor, Fixed Comp. 22K, 1/4W, 5%	AB	RC07GF223J	2	Ref.
A35R10	Resistor, Fixed Comp. 1.8K, 1/4W, 5%	AB	RC07GF182J	1	Ref.
A35R11, 26	Resistor, Fixed Comp. 2.7K, 1/4W, 5%	AB	RC07GF272J	2	Ref.
A35R14	Resistor, Fixed Comp. 33 ohm, 1/4W, 5%	AB	RC07GF330J	1	Ref.
A35R15, 34	Resistor, Fixed Comp. 1.5K, 1/4W, 5%	AB	RC07GF152J	2	Ref.
A35R17, 20, 45	Resistor, Fixed Comp. 12K, 1/4W, 5%	AB	RC07GF123J	3	Ref.
A35R19	Resistor, Fixed Comp. 47K, 1/4W, 5%	AB	RC07GF473J	1	Ref.
A35R23	Resistor, Fixed Comp. 15 ohm, 1/4W, 5%	AB	RC07GF150J	1	1
A35R24	Resistor, Fixed Comp. 4.7K, 1/4W, 5%	AB	RC07GF472J	1	Ref.
A35R28	Resistor, Fixed Comp. 47 ohm, 1/4W, 5%	AB	RC07GF470J	1	Ref.
A35R30, 41	Resistor, Fixed Comp. 15K, 1/4W, 5%	AB	RC07GF153J	2	Ref.
A35R33	Resistor, Fixed Comp. 150 ohm, 1/4W, 5%	AB	RC07GF151J	1	Ref.
A35R35	Resistor, Fixed Comp. 18K, 1/4W, 5%	AB	RC07GF183J	1	Ref.

RESET CIRCUIT PARTS LIST (Cont.)

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A35R36	Resistor, Fixed Comp. 390 ohm, 1/4W, 5%	AB	RC07GF391J	1	Ref.
A35R37	Resistor, Fixed Comp. 4.7 ohm, 1/4W, 5%	AB	RC07GF4R7J	1	1
A35R38	Resistor, Fixed Comp. 10 ohm, 1/4W, 5%	AB	RC07GF100J	1	3
A35R39	Resistor, Fixed Comp. 56K, 1/4W, 5%	AB	RC07GF563J	1	Ref.
A35R42	Resistor, Fixed Comp. 1 meg, 1/4W, 5%	AB	RC07GF105J	1	1
A35S1	Switch, Slide DPDT	CW	G-126	1	1
A35TP1	Connector, Test Point	CAM	1597-2	1	Ref.

R AND C CIRCUIT PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A36	R & C Circuit PCB Assembly	EE	10-3988C		1
A36C1	Capacitor, Dipped Mica 120 pf, 500 wvdc, 5%	SAN	D155F121J0	1	Ref.
A36C2, 13, 18	Capacitor, Dipped Mica 1000 pf, 100 wvdc, 5%	SAN	D151F102J0	3	Ref.
A36C3, 10, 12, 17, 15	Capacitor, Ceramic Disc .005 uf, 50 wvdc	SPR	TG-D50	5	Ref.
A36C4, 7	Capacitor, Dipped Mica 150 pf, 500 wvdc, 5%	SAN	D155F151J0	2	2
A36C5, 6, 8, 9	Capacitor, Dipped Mica 22 pf, 500 wvdc, 5%	SAN	D155F220J0	4	Ref.
A36C11, 19-22	Capacitor, Plastic Film .1 uf, 250 wvdc	SIE	B32-232-S3104	5	Ref.
A36C14	Capacitor, Dipped Mica 220 pf, 500 wvdc, 5%	SAN	D155F221J0	1	Ref.
A36C16	Capacitor, Dipped Mica 47 pf, 500 wvdc, 5%	SAN	D155F470J0	1	Ref.
A36C23	Capacitor, Dipped Mica 180 pf, 500 wvdc, 5%	SAN	D155F181J0	1	Ref.
A36CR1, 2, 4-14	Diode	CDC	CD6267	13	Ref.
A36J1	Connector	SEA	51-028-000	1	1
A36J2	Connector	SEA	55-039-000	1	1
A36Q1-4, 8-11	Transistor	EE	4-1003	8	Ref.
A36Q5-7	Transistor	CML	2N708	3	Ref.
A36Q12	Transistor	MOT	MPS3640	1	Ref.
A36R1, 3	Resistor, Fixed Comp. 2.7K, 1/4W, 5%	AB	RC07GF272J	2	Ref.
A36R2	Resistor, Fixed Comp. 2.2K, 1/4W, 5%	AB	RC07GF222J	1	Ref.
A36R4, 19	Resistor, Fixed Comp. 10 ohm, 1/4W, 5%	AB	RC07GF100J	2	7

R AND C CIRCUIT PARTS LIST (Cont.)

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A36R5, 13, 14, 20, 51	Resistor, Fixed Comp. 3.3K, 1/4W, 5%	AB	RC07GF332J	5	Ref.
A36R6	Resistor, Fixed Comp. 6.8K, 1/4W, 5%	AB	RC07GF682J	1	Ref.
A36R7	Resistor, Fixed Comp. 470 ohm, 1/4W, 5%	AB	RC07GF471J	1	Ref.
A36R8	Not Used				
A36R9, 18, 21, 43, 50	Resistor, Fixed Comp. 270 ohm, 1/4W, 5%	AB	RC07GF271J	5	Ref.
A36R10	Resistor, Fixed Comp. 47K, 1/4W, 5%	AB	RC07GF473J	1	Ref.
A36R11	Not Used				
A36R12, 16	Resistor, Fixed Comp. 12K, 1/4W, 5%	AB	RC07GF123J	2	Ref.
A36R15, 17, 25	Resistor, Fixed Comp. 820 ohm, 1/4W, 5%	AB	RC07GF821J	3	Ref.
A36R22, 29, 33, 45	Resistor, Fixed Comp. 47 ohm, 1/4W, 5%	AB	RC07GF470J	4	Ref.
A36R23	Resistor, Fixed Comp. 220 ohm, 1/4W, 5%	AB	RC07GF221J	1	Ref.
A36R24, 40, 42, 44	Resistor, Fixed Comp. 27K, 1/4W, 5%	AB	RC07GF273J	4	Ref.
A36R26	Resistor, Fixed Comp. 68 ohm, 1/4W, 5%	AB	RC07GF680J	1	1
A36R27	Resistor, Fixed Comp. 22 ohm, 1/4W, 5%	AB	RC07GF220J	1	1
A36R28	Resistor, Fixed Comp. 470 ohm, 1/2W, 5%	AB	RC20GF471J	1	Ref.
A36R30	Resistor, Fixed Comp. 1.8K, 1/4W, 5%	AB	RC07GF182J	1	Ref.
A36R31	Not Used				
A36R32, 35	Resistor, Fixed Comp. 680 ohm, 1/4W, 5%	AB	RC07GF681J	2	Ref.

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A36R34, 47, 48	Resistor, Fixed Comp. 1.5K, 1/4W, 5%	AB	RC07GF152J	3	Ref.
A36R36, 41,	Resistor, Fixed Comp. 1.2K, 1/4W, 5%	AB	RC07GF122J	2	Ref.
A36R37, 39, 53	Resistor, Fixed Comp. 10K, 1/4W, 5%	AB	RC07GF103J	3	Ref.
A36R38	Resistor, Fixed Comp. 4.7K, 1/4W, 5%	AB	RC07GF472J	1	Ref.
A36R46	Resistor, Fixed Comp. 560 ohm, 1/4W, 5%	AB	RC07GF561J	1	1
A36R54	Resistor, Fixed Comp. 100 ohm, 1/4W, 5%	AB	RC07GF101J	1	Ref.
A36R55	Resistor, Fixed Comp. 5.6K, 1/4W, 5%	AB	RC07GF562J	1	Ref.
A36TP1-3	Connector, Test Point	CAM	1597-2	3	Ref.
A36W1	Cable, Coax	CML	RG188/U	2-7/8"	2-7/8"
A36W2	Cable, Coax	CML	RG188/U	14"	14"

TIME BASE DELAY CIRCUIT PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A37	Time Base Delay PCB Assembly	EE	10-3981A		1
A37C1	Capacitor, Mylar Micro-flat 2700 pf, 50 wvdc, 5%	GE	65F10C-272	1	1
A37C2, 12	Capacitor, Plastic Film .01 uf, 400 wvdc, 20%	SIE	B32-232-A6103M	2	Ref.
A37C3	Capacitor, Electrolytic 50 uf, 25 wvdc	SPR	TE1209	1	1
A37C4	Capacitor, Electrolytic 10 uf, 25 wvdc	SPR	TE1204	1	1
A37C5	Not Used				
A37C6, 9, 10	Capacitor, Dipped Mica 1000 pf, 100 wvdc, 5%	SAN	D151F102J0	3	Ref.
A37C7, 8	Capacitor, Dipped Mica 470 pf, 500 wvdc, 5%	SAN	D155F471J0	2	Ref.
A37C11	Capacitor, Dipped Mica 560 pf, 500 wvdc, 5%	SAN	D155F561J0	1	1
A37CR1, 4, 5, 7, 9-12, 15.	Diode	EE	3-1001	9	Ref.
A37CR8	Diode	SEM	SC2	1	3
A37CR13	Diode	CDC	CD6267	1	Ref.
A37L1	Inductor, 10 uh	DEC	1537-36	1	1
A37Q1, 2, 4	Transistor	CML	2N3702/2N3638	3	Ref.
A37Q3	Transistor	CML	2N3053	1	7
A37Q5, 6	Transistor	CML	2N404	2	Ref.
A37Q7	Transistor	EE	4-1003	1	Ref.
A37Q8	Transistor	CML	2N3702	1	Ref.
A37R1, 23, 24	Resistor, Fixed Comp. 470 ohm, 1/4W, 5%	AB	RC07GF471J	3	Ref.
A37R2	Resistor, Fixed Comp. 150K, 1/4W, 5%	AB	RC07GF154J	1	1
A37R3	Resistor, Fixed Comp. 15K, 1/4W, 5%	AB	RC07GF153J	1	Ref.
A37R4	Resistor, Fixed Comp. 6.8K, 1/4W, 5%	AB	RC07GF682J	1	Ref.
A37R5	Resistor, Fixed Comp. 10 ohm, 1/4W, 5%	AB	RC07GF100J	1	Ref.

TIME BASE DELAY CIRCUIT PARTS LIST (Cont.)

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A37R6	Resistor, Fixed Comp. 1.5K, 1/4W, 5%	AB	RC07GF152J	1	Ref.
A37R7, 21, 22	Resistor, Fixed Comp. 2.7K, 1/4W, 5%	AB	RC07GF272J	3	Ref.
A37R8	Resistor, Fixed Comp. 47 ohm, 1/4W, 5%	AB	RC07GF470J	1	Ref.
A37R9, 31	Resistor, Fixed Comp. 1K, 1/4W, 5%	AB	RC07GF102J	2	Ref.
A37R10-11	Not Used				
A37R12	Resistor, Fixed Comp. 100 ohm, 1/4W, 5%	AB	RC07GF101J	1	Ref.
A37R13	Resistor, Fixed Comp. 1 ohm, 1/2W, 5%	AB	RC20GF1R0J	1	1
A37R14, 28	Resistor, Fixed Comp. 1.8K, 1/4W, 5%	AB	RC07GF182J	2	Ref.
A37R15, 18, 25-27	Resistor, Fixed Comp. 10K, 1/4W, 5%	AB	RC07GF103J	5	Ref.
A37R16-17	Not Used				
A37R19-20	Resistor, Fixed Comp. 22K, 1/4W, 5%	AB	RC07GF223J	2	Ref.
A37R29	Resistor, Fixed Comp. 47K, 1/4W, 5%	AB	RC07GF473J	1	Ref.
A37R30	Resistor, Fixed Comp. 220 ohm, 1/2W, 5%	AB	RC20GF221J	1	Ref.

POWER SUPPLY PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A47	Power Supply Assembly	EE	10-3956B		1
A47C1, 2	Capacitor, Electrolytic 4500 uf, 25 wvdc	SAN	505-3837-02	2	2
A47C3	Capacitor, Dual Electrolytic 2 x 4500 uf, 15 & 25 wvdc	SAN	505-2619-02	1	1
A47C4	Capacitor, Dual Electrolytic 2 x 500 uf, 50 wvdc	SAN	505-1420-02	1	1
A47C5	Capacitor, Dual Electrolytic 2 x 20 uf, 450 wvdc	SAN	505-1212-02	1	1
A47C6	Capacitor, Electrolytic 1500 uf, 65 wvdc	SAN	505-3817-02	1	1
A47C7-8	Capacitor, Electrolytic 500 uf, 30 wvdc	SPR	39507G030FL4	2	2
A47C9	Capacitor, Plastic Film .1 uf, 250 wvdc	SIE	B32-232-S3104	1	Ref.
A47CR1-5	Not Used				
A47CR6-12, 16	Diode	SOL	2A100	8	8
A47CR13	Diode	SEM	SC-8	1	1
A47CR14-15	Diode	SEM	SC-2	2	Ref.
A47CR17	Diode, Zener	CDC	1N759A	1	1
A47CR18	Diode, Zener (option P only)	MOT	1N3005A	1	1
A47F1, 2, 4	Fuse, 2 A F B	LIT	3AG	3	3
A47F3	Fuse, 3 A F B	LIT	3AG	1	1
A47J1	Connector, 18 pin	CIJ	250-18-70-170	1	1
A47MP1	Clamp-Crystal	AUG	168T1-183H	1	1
A47Q1-4	Transistor	RCA	40251	4	4
A47R1-37	Not Used				
A47R38, 40	Resistor, Fixed Comp. 330 ohm, 1/2W, 5%	AB	RC20GF331J	2	2
A47R39, 41, 42, 46, 47	Resistor, Fixed Comp. 10K, 1/2W, 5%	AB	RC20GF103J	5	Ref.
A47R43, 49	Resistor, Fixed Comp. 390 ohm, 1/2W, 5%	AB	RC20GF391J	2	3

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A47R44	Resistor, Fixed Comp. 330K, 1/2W, 5%	AB	RC20GF334J	1	1
A47R45	Resistor, Fixed Comp. 470 ohm, 2W, 5%	AB	RC42GF471J	1	1
A47R48	Resistor, Fixed Comp. 470 ohm, 1/2W, 5%	AB	RC20GF471J	1	2
A47R50	Resistor, Wire Wound (option P only) 8K, 20W, 5%	IRC	2C-8000	1	1
A47R51	Resistor, Fixed Comp. (option P only) 820 ohm, 2W, 5%	AB	RC42GF821J	1	1
A47T1	Transformer	EE	21-3935	1	1
A47XF1-4	Holder, Fuse	LIT	342014-4KP	4	4
A47XY1	Socket, crystal	CIJ	8AM	1	1
A47X1	Crystal, 1 MHz	OVN	OSC-11-14	1	1

POWER SUPPLY REGULATOR PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A47A1	P.S. Regulator PCB Assembly	EE	10-3980E		1
A47A1C1-10	Not Used				
A47A1C11-15	Capacitor, Tantalum Electrolytic .47 uf, 35 wvdc	SPR	150D474X00-35A2	5	5
A47A1C16	Capacitor, Tantalum Electrolytic 2.2 uf, 20 wvdc	SPR	150D225X00-20A2	1	1
A47A1CR1, 4	Diode	EE	3-1001	2	Ref.
A47A1CR2	Diode, Zener	CDC	1N752A	1	1
A47A1CR3	Diode	MOT	1N3031	1	1
A47A1CR5	Diode	TRS	S570G	1	Ref.
A47A1Q1-2	Transistor	CML	2N1304	2	2
A47A1Q3, 9	Transistor	CML	2N2924	2	2
A47A1Q4, 5, 8, 11, 14	Transistor	CML	2N3053	5	Ref.
A47A1Q6, 7, 12, 13	Transistor	CML	2N404	4	Ref.
A47A1Q10	Transistor	CML	2N3638	1	Ref.
A47A1R1-4	Resistor, Variable 500 ohm, Wire Wound	CTS	BC35547	4	4
A47A1R5	Resistor, Fixed Comp. 10K, 1/4W, 5%	AB	RC07GF103J	1	Ref.
A47A1R6, 15	Resistor, Fixed Comp. 1K, 1/4W, 5%	AB	RC07GF102J	2	Ref.
A47A1R7, 14, 47	Resistor, Metal Film 464 ohm, 1/2W, 1%	IRC	RN65-TO	3	3
A47A1R8	Resistor, Metal Film 100 ohm, 1/4W, 1%	IRC	RN60-TO	1	1
A47A1R9, 23, 26, 28, 33	Resistor, Fixed Comp. 100 ohm, 1/4W, 5%	AB	RC07GF101J	5	Ref.
A47A1R10	Not used				
A47A1R11, 32, 36	Resistor, Fixed Comp. 1.5K, 1/4W, 5%	AB	RC07GF152J	3	Ref.
A47A1R12	Resistor, Fixed Comp. 270 ohm, 1/4W, 5%	AB	RC07GF271J	1	Ref.

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A47A1R13, 35	Resistor, Fixed Comp. 12K 1/4W, 5%	AB	RC07GF123J	2	Ref.
A47A1R16, 27	Resistor, Fixed Comp. 680 ohm, 1/2W, 5%	AB	RC20GF681J	2	2
A47A1R17	Resistor, Fixed Comp. 1.8K, 1/4W, 5%	AB	RC07GF182J	1	Ref.
A47A1R18	Resistor, Fixed Comp. 5.6K, 1/4W, 5%	AB	RC07GF562J	1	Ref.
A47A1R19	Resistor, Fixed Comp. 180 ohm, 1/4W, 5%	AB	RC07GF181J	1	1
A47A1R20, 21, 29	Resistor, Fixed Comp. 270 ohm, 1/2W, 5%	AB	RC20GF271J	3	3
A47A1R22	Resistor, Fixed Comp. 390 ohm, 1/2W, 5%	AB	RC20GF391J	1	1
A47A1R24	Resistor, Fixed Comp. 2.7K, 1/4W, 5%	AB	RC07GF272J	1	Ref.
A47A1R25	Resistor, Fixed Comp. 220 ohm, 1/2W, 5%	AB	RC20GF221J	1	1
A47A1R30	Resistor, Fixed Comp. 2.2K, 1/4W, 5%	AB	RC07GF222J	1	Ref.
A47A1R31	Resistor, Fixed Comp. 150 ohm, 1/4W, 5%	AB	RC07GF151J	1	Ref.
A47A1R34, 37	Resistor, Fixed Comp. 820 ohm, 1/4W, 5%	AB	RC07GF821J	2	Ref.
A47A1R38	Not Used				
A47A1RX	Resistor, Fixed Comp. 1.2K, 1/4W, 5%	AB	RC07GF122J	1	Ref.

FRONT PANEL PARTS LIST (945/950)

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A48	Front Panel Assembly	EE			
A48C1	Capacitor, Ceramic Disc. .01 uf, 50 wvdc	SPR	TG-S10	1	Ref.
A48I1-4	Lamp	GE	327	4	4
A48J1	Connector, Probe (option P only)	BEN	10-243053-45	1	1
A48MP1	Knob, Range Switch	RAY	G70-3-2G	1	1
A48MP2-6	Knob, Controls	RAY	G70-1-26	4	4
A48MP7	Window, Clear	EE	5-3837-1	1	1
A48MP8	Window, Polascreen	EE	5-3837-2	1	1
A48R1	Resistor, Fixed Comp. 4.7K, 1/4W, 5%	AB	RC07GF472J	1	Ref.
A48R2	Resistor, Fixed Comp. 100K, 1/2W, 5%	AB	RC20GF104J	1	1
A48R3	Resistor, Variable 500 ohm, 5 turns 1.5W	BRNS	3520S-1-501	1	1
A48R4	Resistor, Variable with DPDT Switch 1 meg, 1/4 watt	CTS	39537	1	1
A48R5	Resistor, Variable Dual 1 meg/500 ohm	CTS	301368	1	1
A48R6-7	Resistor, Fixed Comp. 8.2K, 1/2W, 5%	AB	RC20GF822J	2	2
A48R8-9	Resistor, Fixed Comp. 180K, 1W, 5%	AB	RC32GF183J	2	2
A48S1	Switch, Toggle DPST	CH	8370K7	1	1
A48S2	Switch, Push Button	CC	B-2001	1	1
A48S3-4	Switch, Rotary	CTS	54405	2	2
A48S5	Switch, Range	EE	10-3312	1	1
A48XI1-2	Socket, Decimal Light	SLO	855S1-W-9STD	2	2
A48XI3	Socket, Overflow #1	SLO	855S1-W-1STD	1	1
A48XI4	Socket, Overflow #2	SLO	855S1-W-2STD	1	1
A48Z1	Divider, Input Power	WIE	2133B	1	1

FRONT PANEL PARTS LIST (946/951)

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
	Front Panel Assembly (946/951) Add the following in addition to the (945/950) Front Panel.				
A48C2	Capacitor, Ceramic Disc .01 uf, 50 wvdc	SPR	TGS10	1	Ref.
A48CR1-5	Diode	EE	3-1001	5	Ref.
A48R10	Resistor, Fixed Comp. 10V, 1/4W, 5%	AB	RC07GF103J	1	Ref.
A48R11	Resistor, Fixed Comp. 3.3K, 1/4W, 5%	AB	RC07GF332J	1	Ref.
A48S6	Switch, Resolution	EE	10-3985A	1	1

REAR PANEL PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A49	Rear Panel Assembly	EE			
A49B1	Fan	HOW	8011	1	1
A49C1-2	Capacitor, Plastic Film .1 uf, 250 wvdc, 20%	SIE	B32-232-S3104	2	Ref.
A49F1	Fuse, 2ASB, 3AG	LIT	313002	1	1
A49FL1	Line Filter, Assy.	EE	10-3451	1	1
A49J1-2	Connector, BNC	AML	UG1094	2	2
A49J3	Connector, 50 pin	AML	57-40500	1	1
A49J4	Connector, 36 pin (option F only)	AML	57-40360	1	1
A49R1	Resistor, Fixed Comp. 1K, 1/2W, 5%	AB	RC20GF102J	1	1
A49R2	Resistor, Fixed Comp. 100 ohm, 1/4W, 5%	AB	RC07GF101J	1	Ref.
A49S1	Switch, Slide DPDT	CW	518	1	1
A49W1	Cord, Power 6 ft.	COR	3598-2	1	1
A49XF1	Holder, Fuse	EE	14-1013	1	1

LOGIC CHASSIS PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A50	Logic Chassis Assembly	EE	10-3445G		
A50C1-20	Capacitor, Plastic Film .1 uf, 250 wvdc, 20%	SIE	B32-232-S3104	20	Ref.
A50C21-24	Capacitor, Electrolytic 50 uf, 12 wvdc	SPR	TE1133	4	4
A50C25-28	Capacitor, Tantalum 33 uf, 20 wvdc	CI	J33	4	4
A50C29-34	Capacitor, Electrolytic 50 uf, 25 wvdc	SPR	TE1209	6	6
A50C35	Capacitor, Tantalum Electrolytic 2.2 uf, 20 wvdc	SPR	150D225X-0020A2	1	Ref.
A50CR1-22	Diode	EE	3-1001	22	Ref.
A50CR23-24	Diode	CDC	CD6267	2	Ref.
A50J1-7, 9, 11, 13, 15, 17, 19, 21, 23-46.	Connector	CIJ	250-18-30-171	37	37
A50J8, 10, 12, 14, 16, 18, 20, 22.	Connector	CIJ	251-18-30-161	8	8
A50R1	Resistor, Fixed Comp. 47K, 1/4W, 5%	AB	RC07GF473J	1	Ref.
A50R2-33, 46-49	Resistor, Fixed Comp. 6.8K, 1/4W, 5%	AB	RC07GF682J	32	Ref.
A50R34	Resistor, Fixed Comp. 10K, 1/4W, 5%	AB	RC07GF103J	1	Ref.
A50R35	Resistor, Fixed Comp. 1.8K, 1/4W, 5%	AB	RC07GF182J	1	Ref.
A50R36	Resistor, Fixed Comp. 390 ohm, 1/4W, 5%	AB	RC07GF391J	1	Ref.
A50R37	Resistor, Fixed Comp. 1.2K, 1/4W, 5%	AB	RC07GF122J	1	Ref.

LOGIC CHASSIS PARTS LIST (Cont.)

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A50R38	Resistor, Fixed Comp. 6.8K, 1/2W, 5%	AB	RC20GF682J	1	Ref.
A50R39	Resistor, Fixed Comp. 330 ohm, 1/4W, 5%	AB	RC07GF331J	1	Ref.
A50R40	Resistor, Fixed Comp. 15K, 1/4W, 5%	AB	RC07GF153J	1	Ref.
A50R41-45	Resistor, Fixed Comp. 8.2K, 1/4W, 5%	AB	RC07GF822J	4	Ref.

ACCESSORIES PARTS LIST

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A51	Shipping Kit	EE	10-3738B		1
A51E1-2	Extender Boards	EE	10-2043	2	2
A51J1	Adapter 3 to 2	COR	228	1	1
A51MP1	Handles	VEM	FCA6	2	2
A51MP2	Rack Ears	EE	5-3740-A	2	2

PROPRIETARY ASSEMBLIES PARTS LIST

The individual components on the proprietary circuits are not identified. These boards are replaced as complete assemblies.

ASSEMBLY	DESCRIPTION	MFR.	MFR. PART NO.	QTY. PER ASSY.	QTY. PER INST.
A1	F.S. Circuit Assy	EE	10-3982		1
A3	I.C. Circuit Assy	EE	10-3994		1
A4	S.C. Circuit Assy	EE	10-3948		1
A5	C.U. Circuit Assy	EE	10-3993		1
A29	Gate and Centering Circuit Assembly	EE	10-3991		1
A31	I.S. Circuit Assy	EE	10-3963		1

WARRANTY

Eldorado instruments are warranted during a period of one year from date of shipment to original purchaser to be free from defects in material and workmanship This warranty does not apply to vacuum tubes or transistors, except as they are warranted by their manufacturers. The liability of Eldorado under this warranty is limited to replacing or repairing any instrument or component thereof which is returned by Buyer at his expense (see Repairs) during such period and which has not been subjected to misuse, neglect, improper installation, repair, alteration, or accident. Eldorado shall have the right of final determination as to the existence and cause of a defect. In no event shall Eldorado be liable for collateral or consequential damages. This warranty is in lieu of any other warranty, express, implied, or statutory, and no agreement extending or modifying it will be binding upon Eldorado unless in writing and signed by a duly authorized officer. THIS WARRANTY IS VOID IF SEAL ON FACTORY SEALED COMPONENTS IS BROKEN.

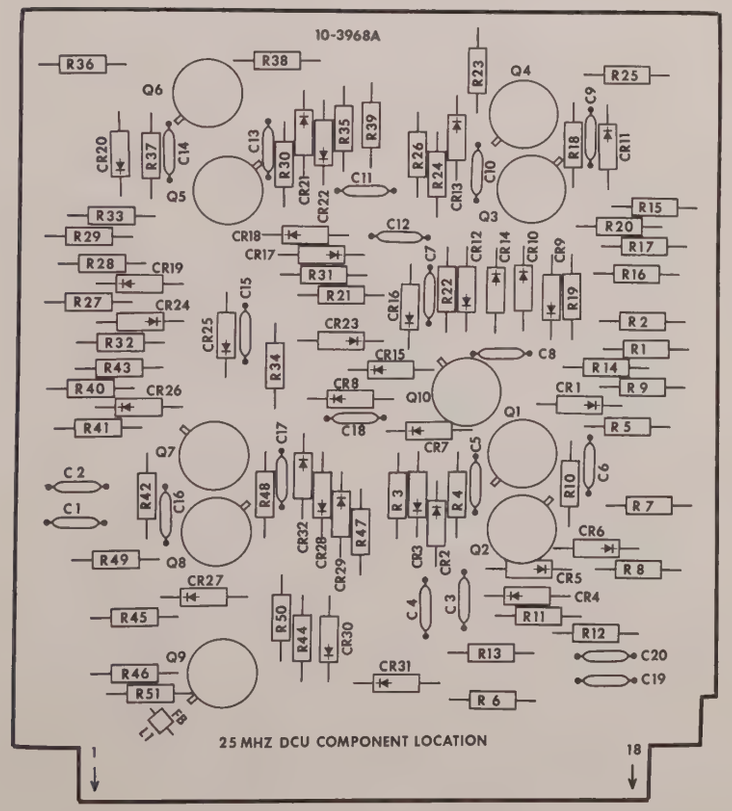
RECEIVING INSPECTION

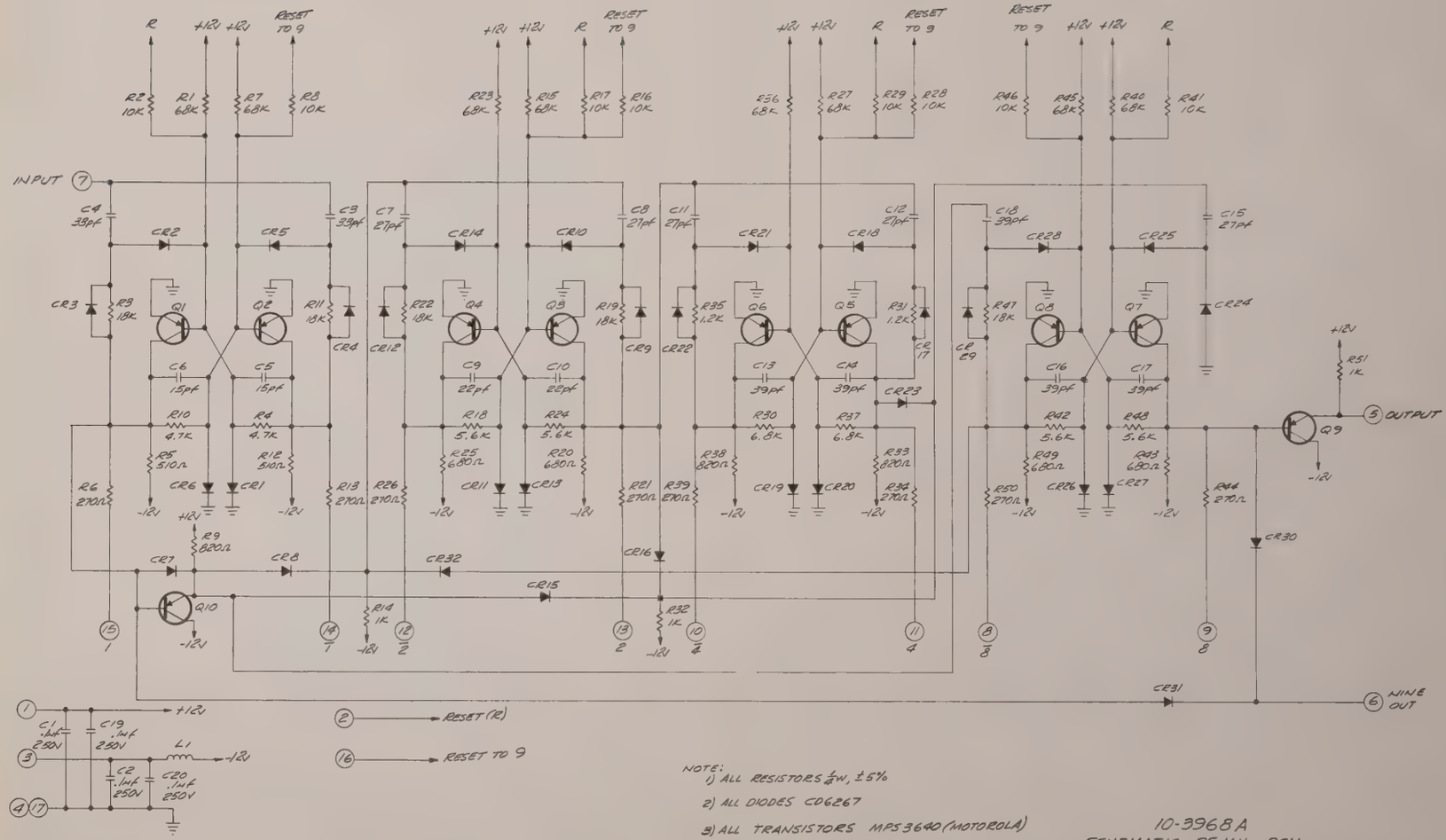
Every Eldorado instrument is carefully inspected and is in perfect working order at the time of shipment. Each instrument should be checked as soon as received. If the instrument or packing case is damaged in any way or fails to operate, a claim should immediately be filed with the transportation company. In any case where damage occurs in transit, Eldorado's obligations under warranty are dependent on the customer's immediately notifying the carrier, so that inspection can be made and a claim filed.

REPAIRS

When an Eldorado instrument requires service, the nearest Eldorado representative should be contacted; all representatives will provide immediate service or arrange factory returns when necessary. In the latter case, the instrument must be dispatched freight prepaid, with insurance coverage arranged by the customer. Freight and insurance on the return trip to the customer will be arranged by Eldorado and charged to the customer.

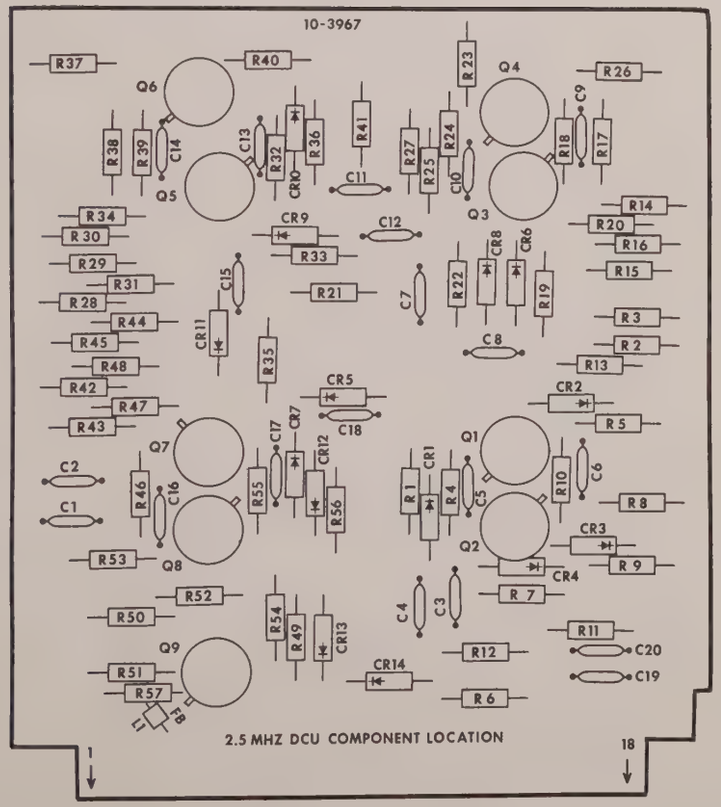
Please specify both model and serial number in all correspondence concerning Eldorado instruments. Address all inquiries regarding Eldorado instruments to your nearest sales representative or Sales Manager, Eldorado Electronics Company, 601 Chalomar Road, Concord, California (94520).

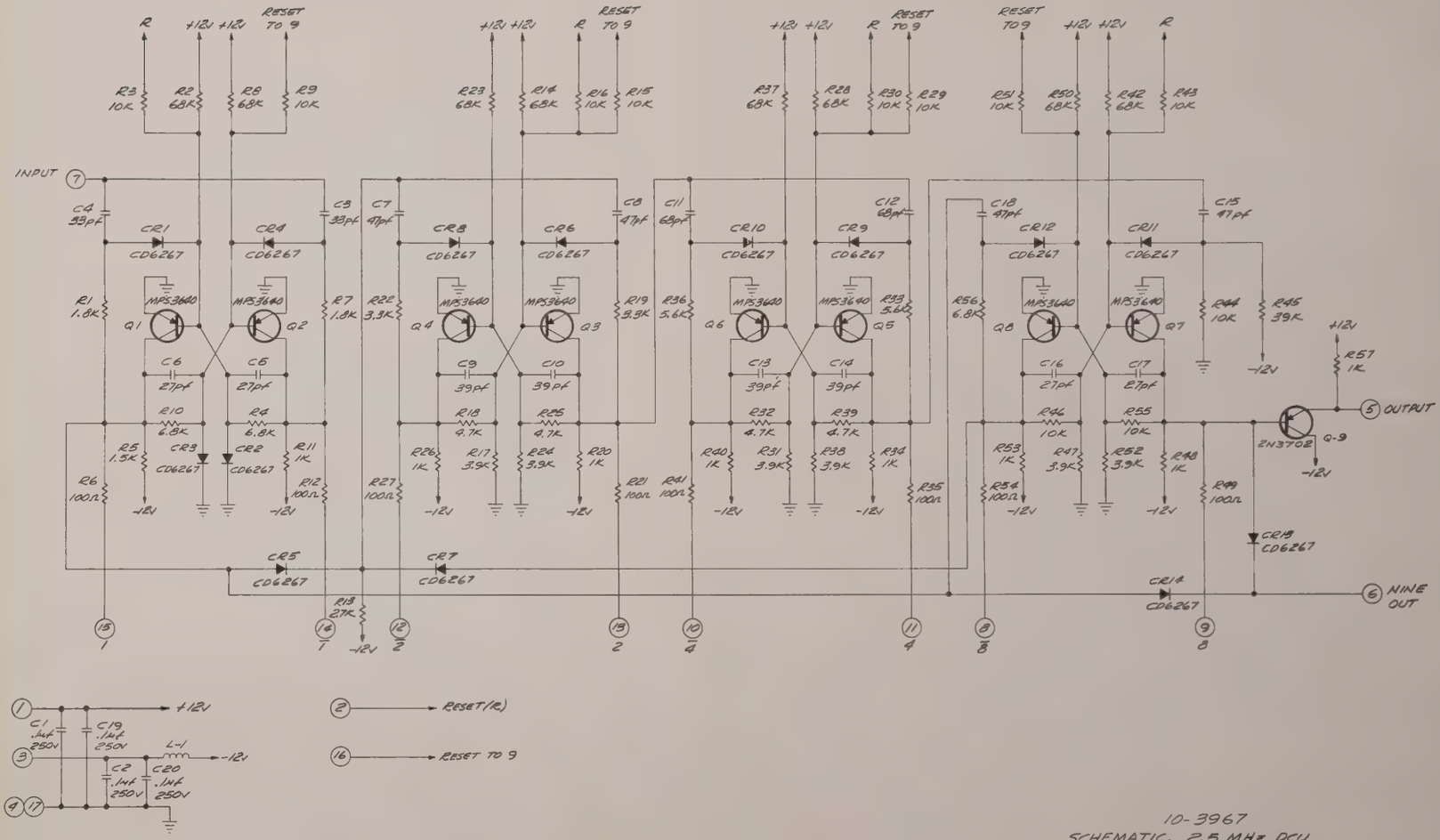




10-3968A
SCHEMATIC, 25 MHz DCU
JAI 3-16-66

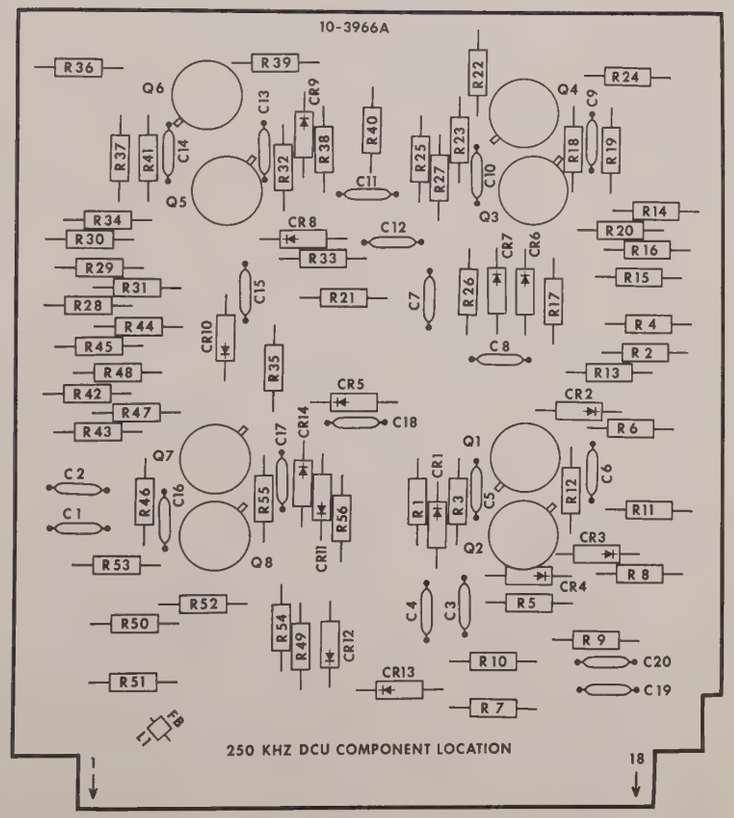
FIGURE 28 25 MHz DECADE COUNTING UNIT
SCHEMATIC DIAGRAM & COMPONENT LOCATION

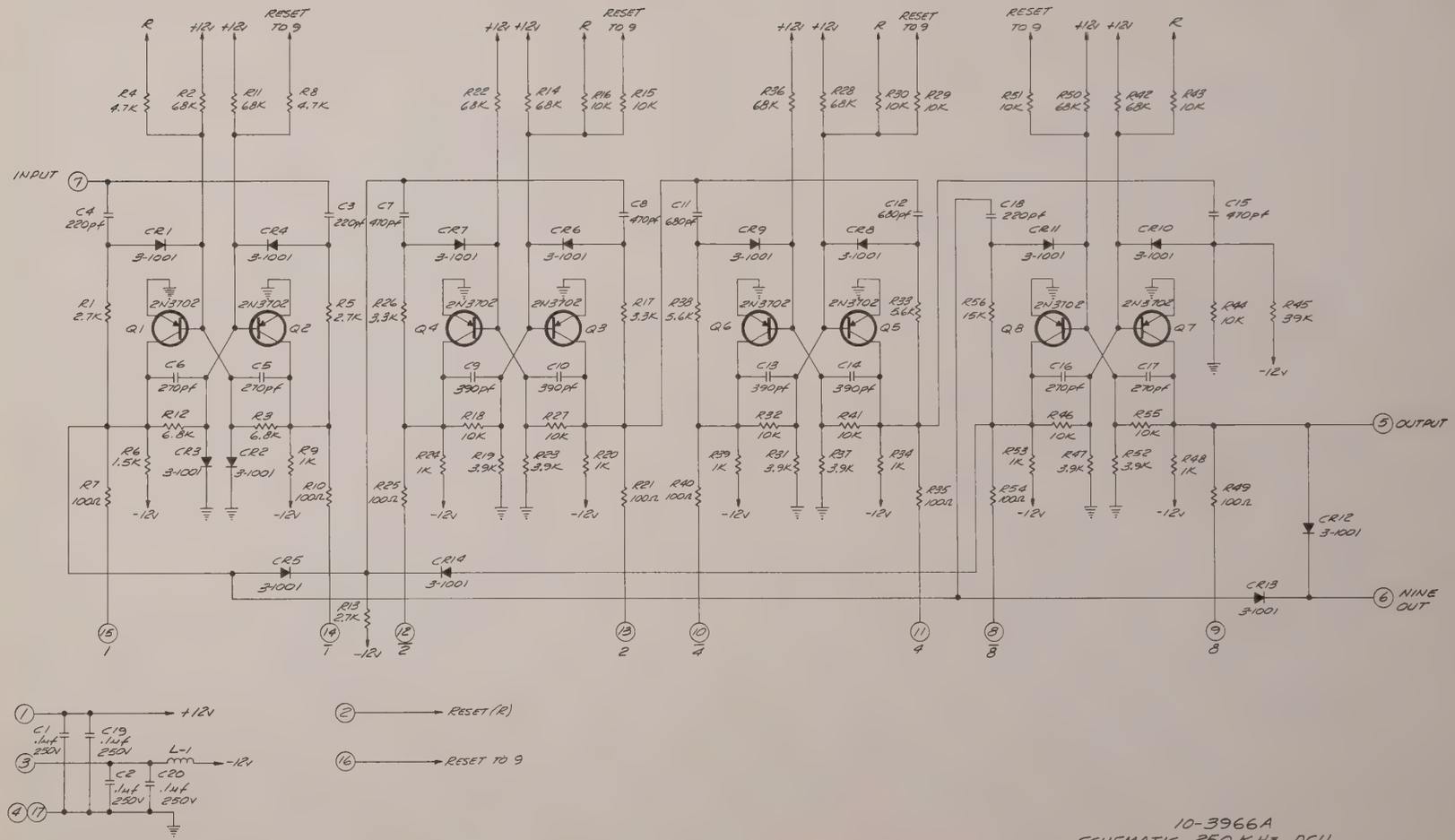




10-3967
SCHEMATIC, 2.5 MHz DCU
JAI 5-12-66

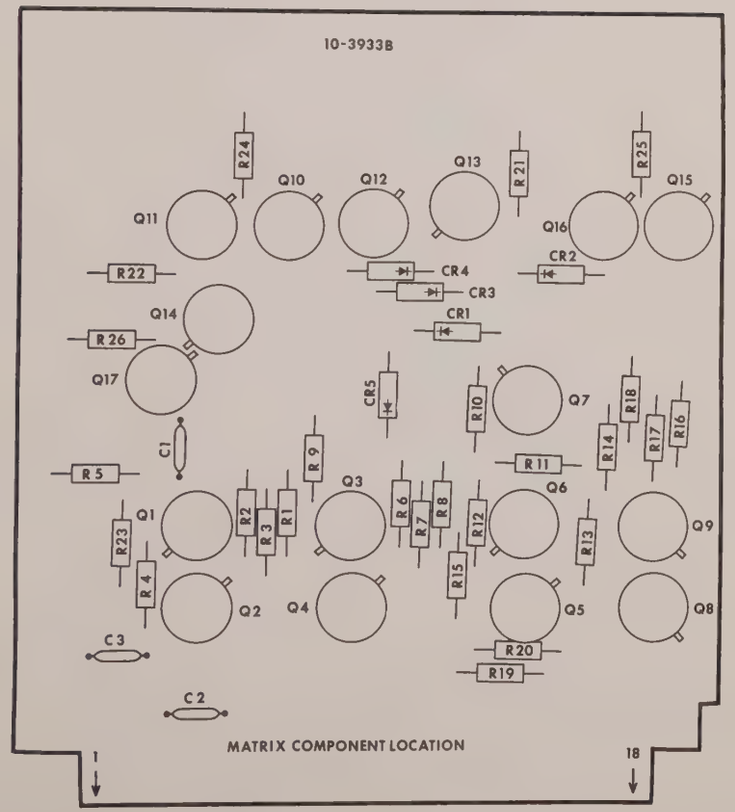
FIGURE 29 2.5 MHz DECADE COUNTING UNIT
SCHEMATIC DIAGRAM & COMPONENT LOCATION

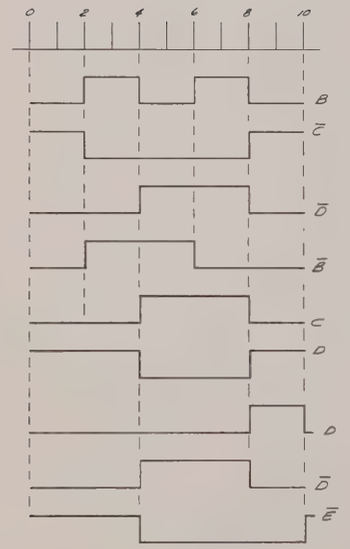




10-3966A
SCHEMATIC, 250 KHz DCU
JAI 5-5-66

FIGURE 30 250 KHz DECADE COUNTING UNIT
SCHEMATIC DIAGRAM & COMPONENT LOCATION





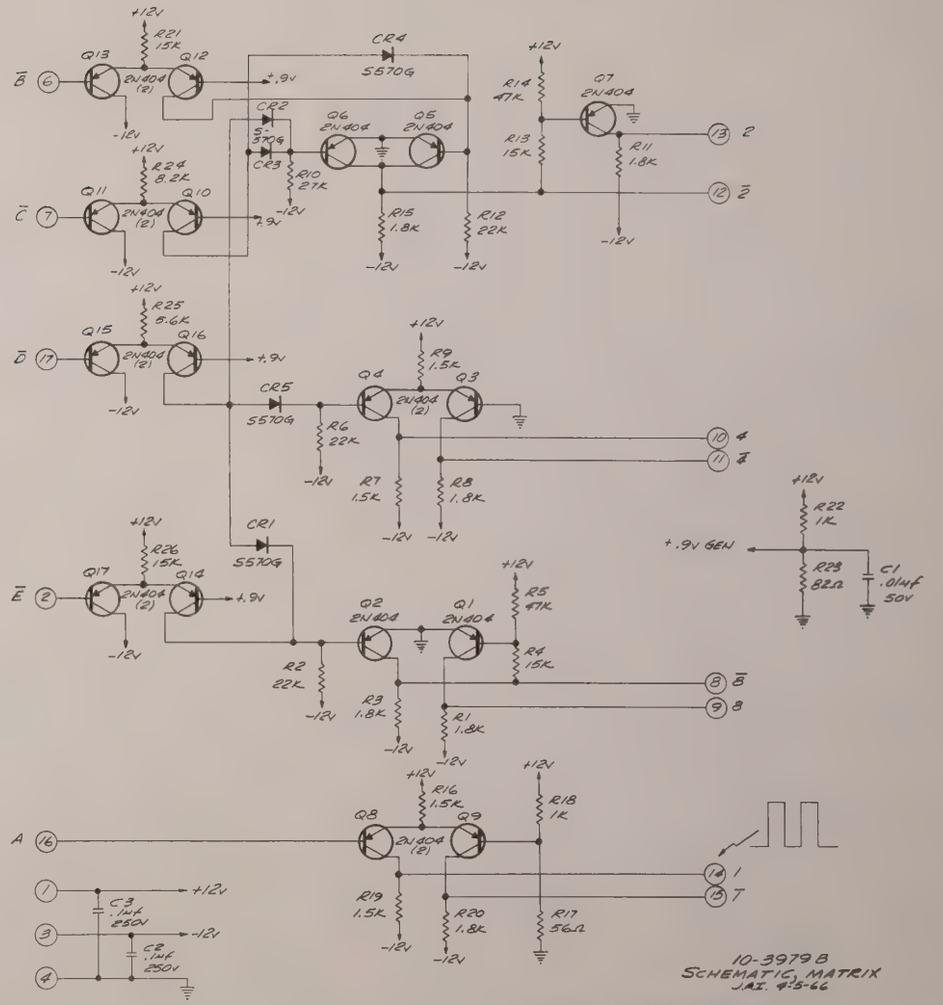
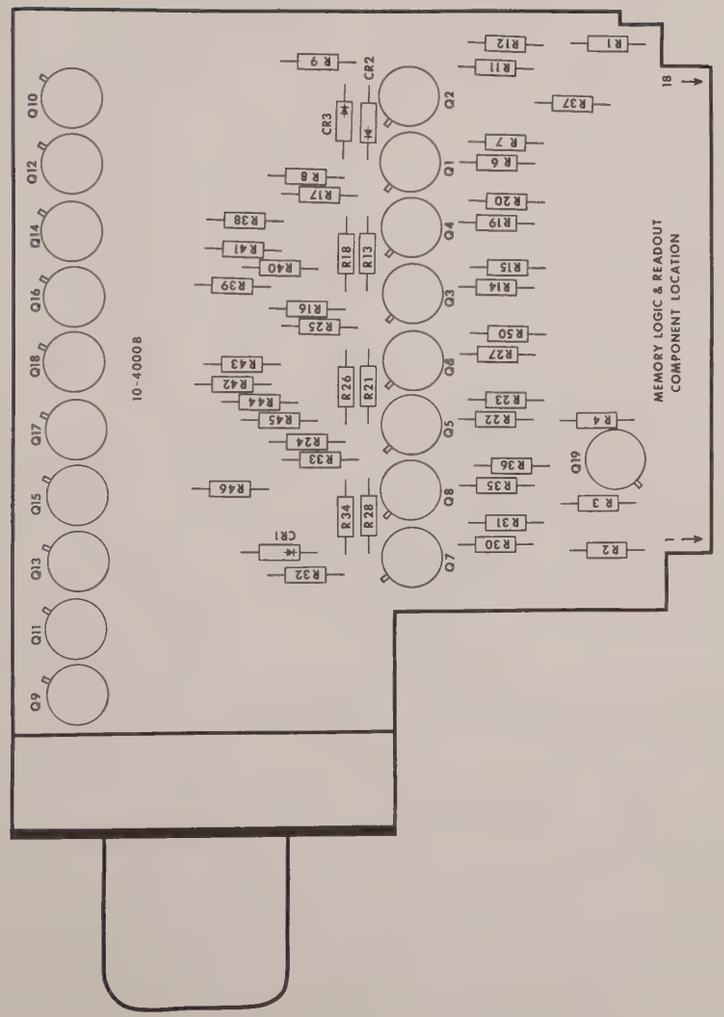
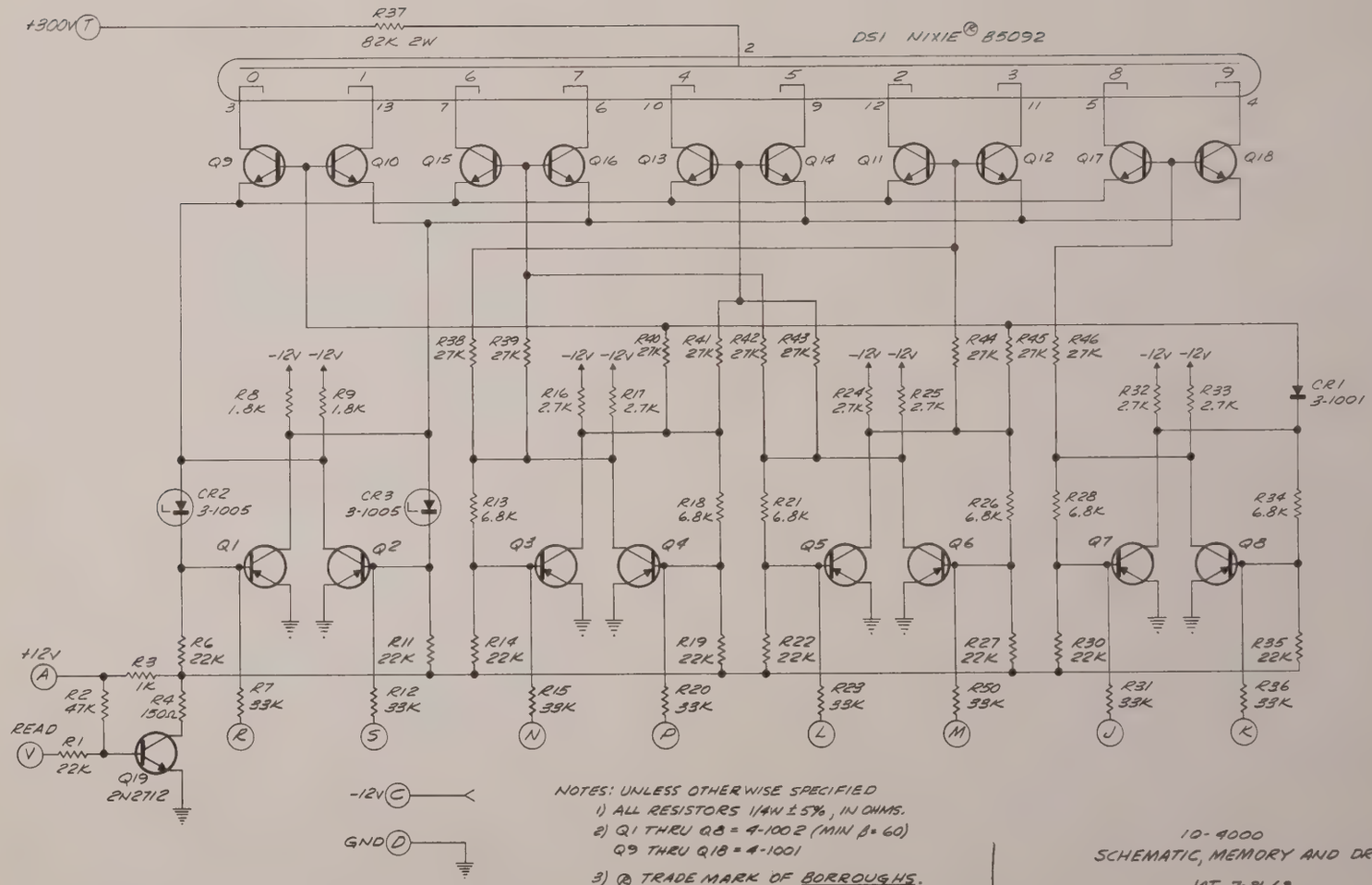


FIGURE 31 MATRIX CIRCUIT
SCHEMATIC DIAGRAM & COMPONENT LOCATION

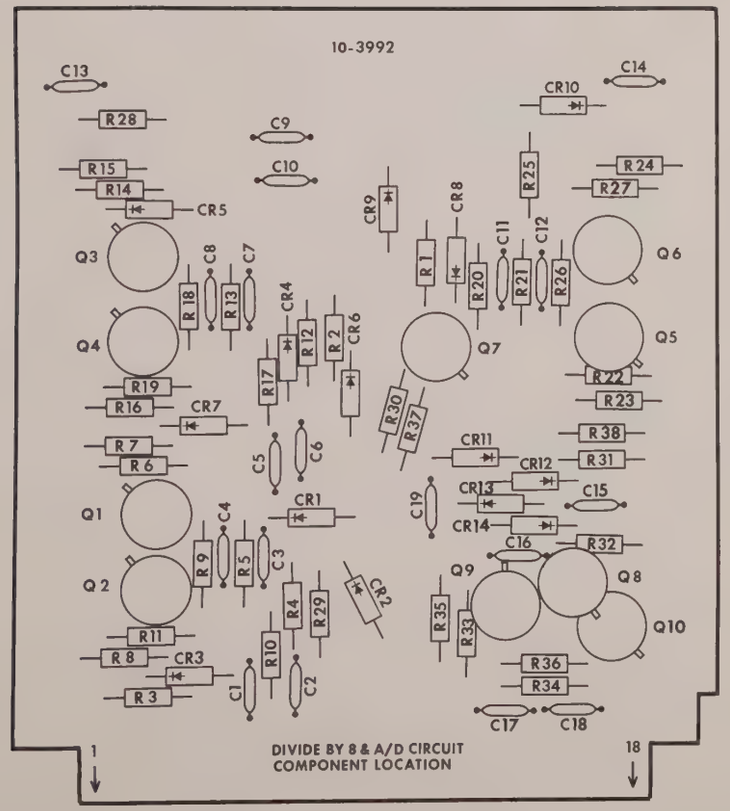


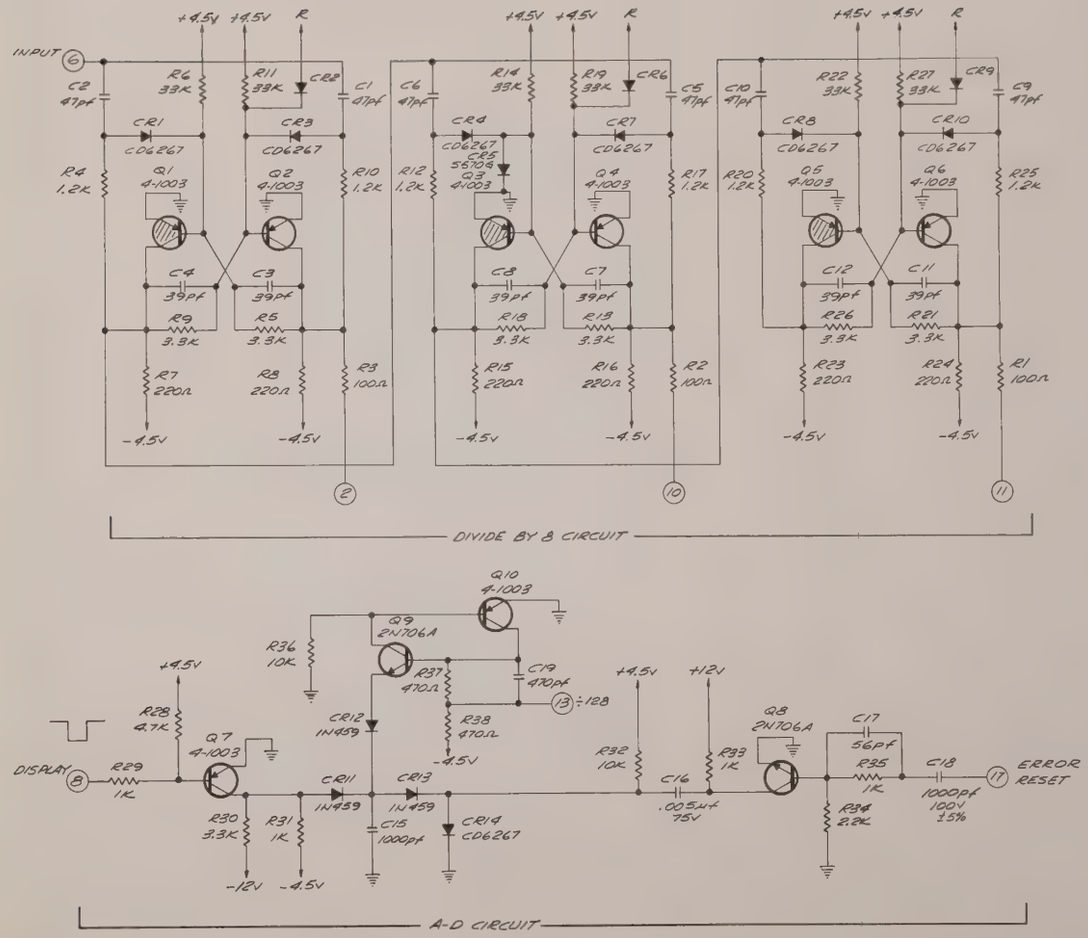


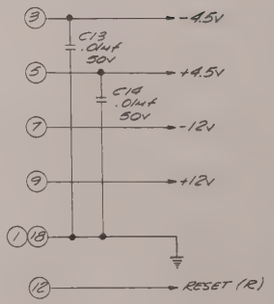
NOTES: UNLESS OTHERWISE SPECIFIED
1) ALL RESISTORS 1/4W ±5%, IN OHMS.
2) Q1 THRU Q8 = 4-1002 (MIN β = 60)
Q9 THRU Q18 = 4-1001
3) ® TRADE MARK OF BORROUGHS.

10-4000
SCHEMATIC, MEMORY AND DRIVER
JAI 7-31-69

FIGURE 32 MEMORY READOUT
SCHEMATIC DIAGRAM & COMPONENT LOCATION

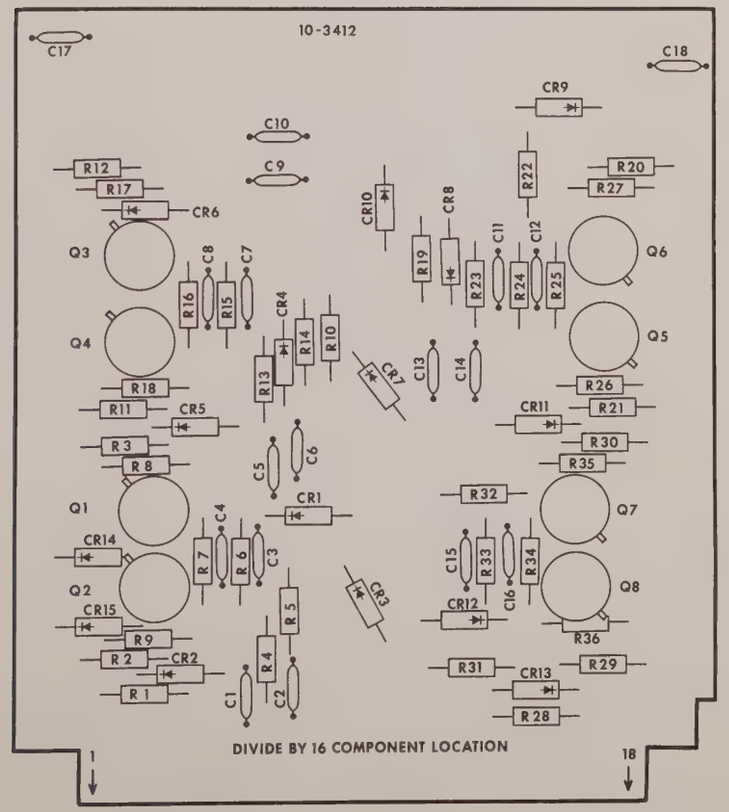


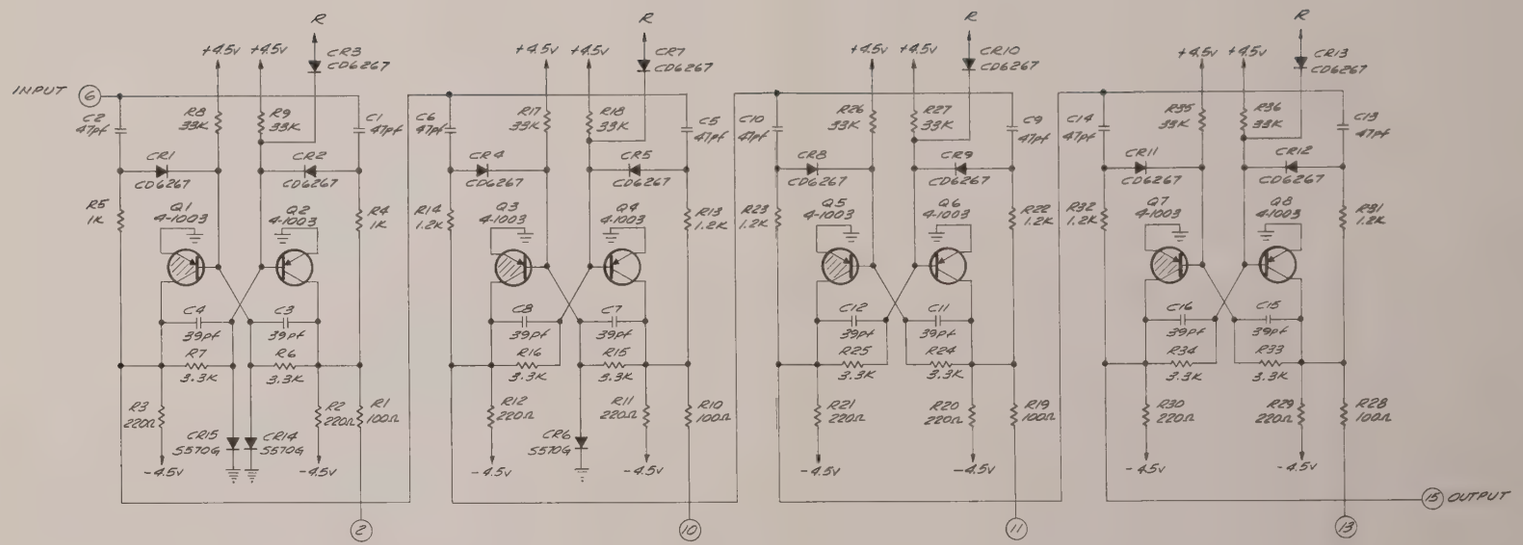




10-3992 A
SCHEMATIC, DIVIDE BY 8 AND A-D CIRCUIT
J.A.I. 9-14-66

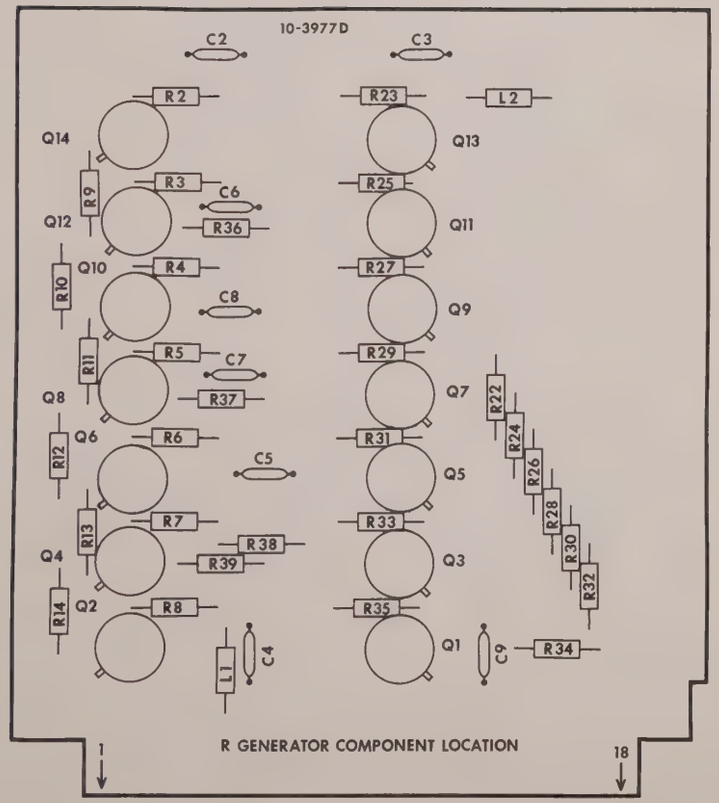
FIGURE 33 A.D. & DIVIDE-BY-EIGHT
SCHEMATIC DIAGRAM & COMPONENT LOCATION

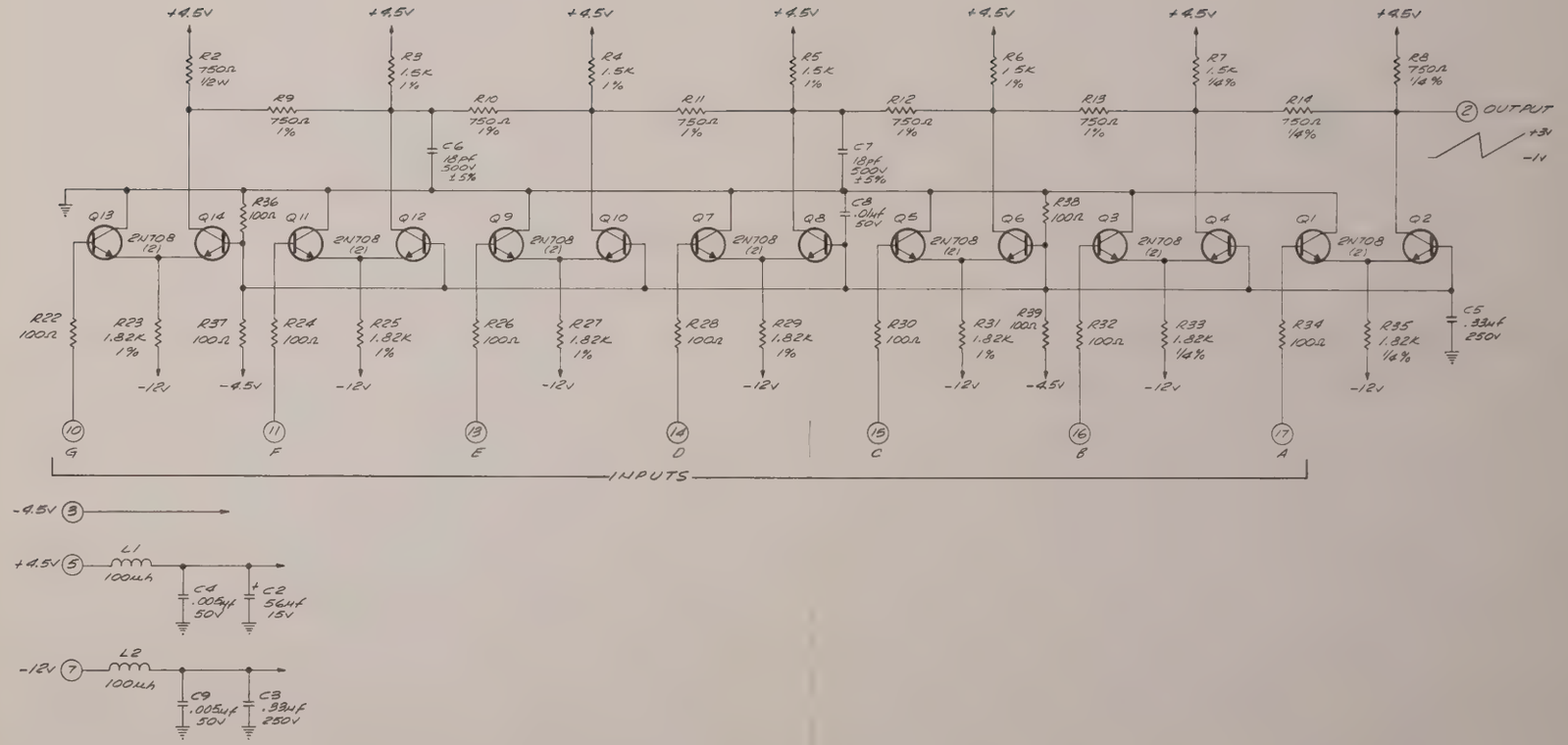




10-3412
SCHEMATIC, ÷16 CU
JAI 5-11-66

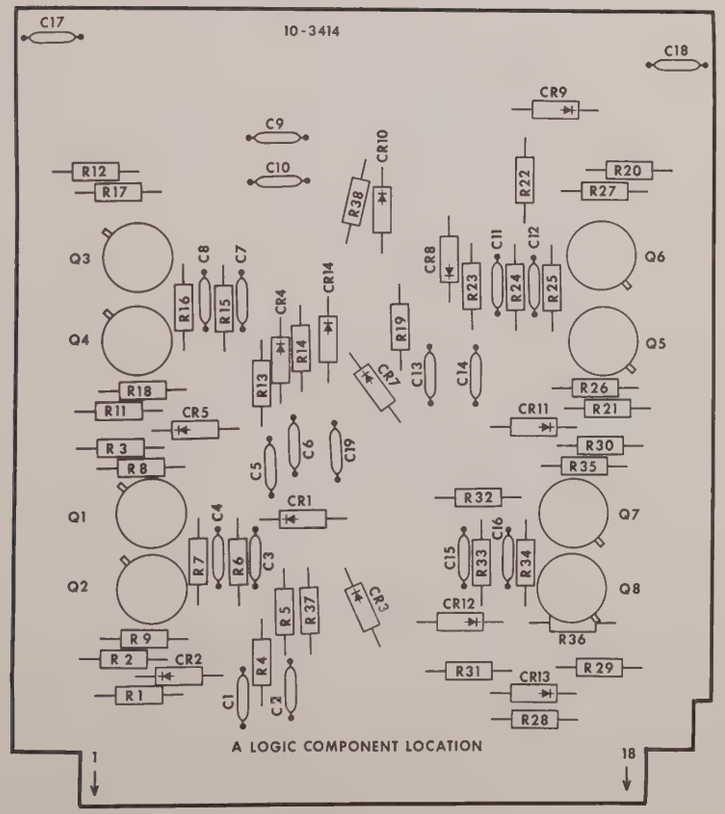
FIGURE 34 DIVIDE-BY-SIXTEEN
SCHEMATIC DIAGRAM & COMPONENT LOCATION

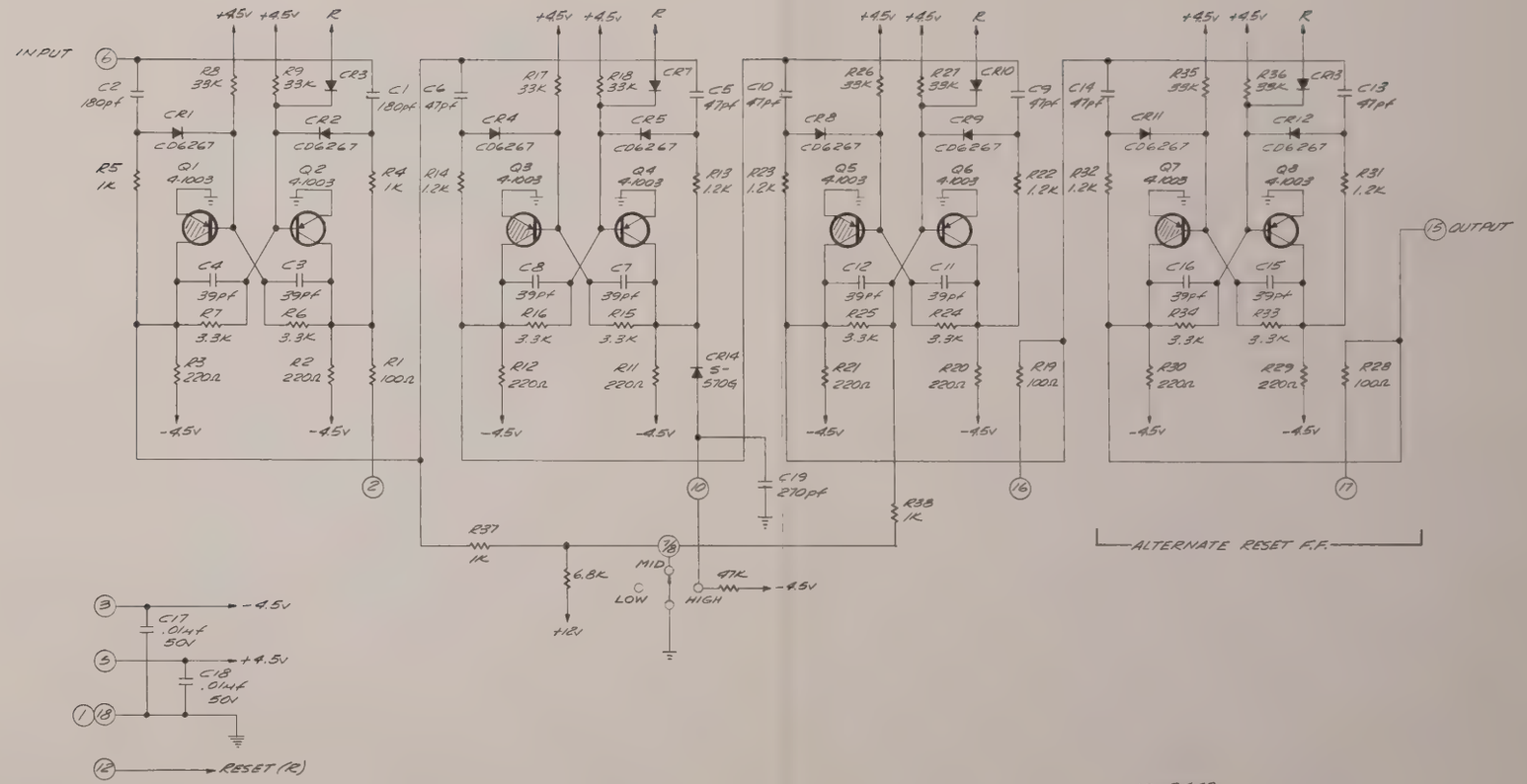




10-3977
SCHEMATIC, RAMP GENERATOR
J.A.I. 4-6-66

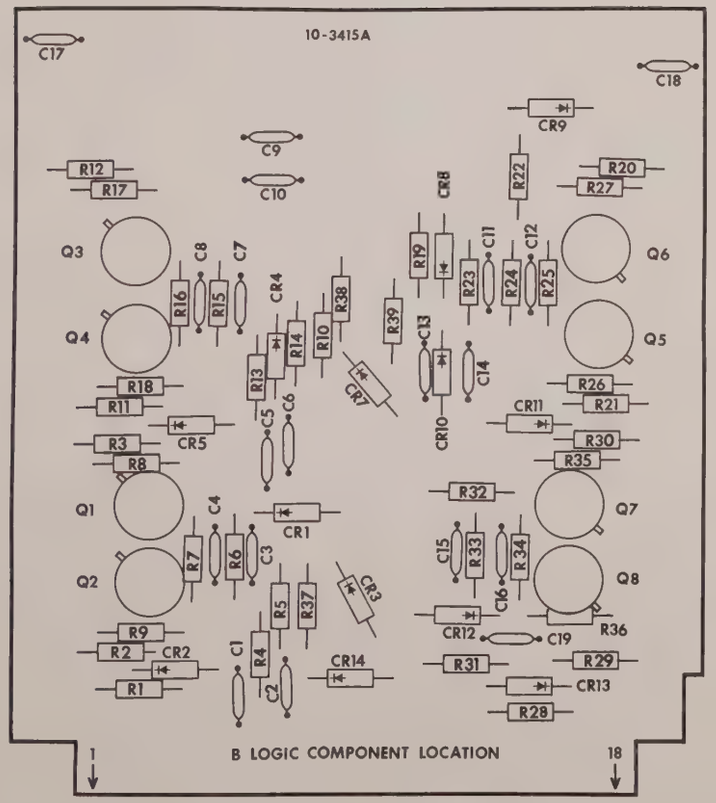
FIGURE 35 RAMP GENERATOR
SCHEMATIC DIAGRAM & COMPONENT LOCATION

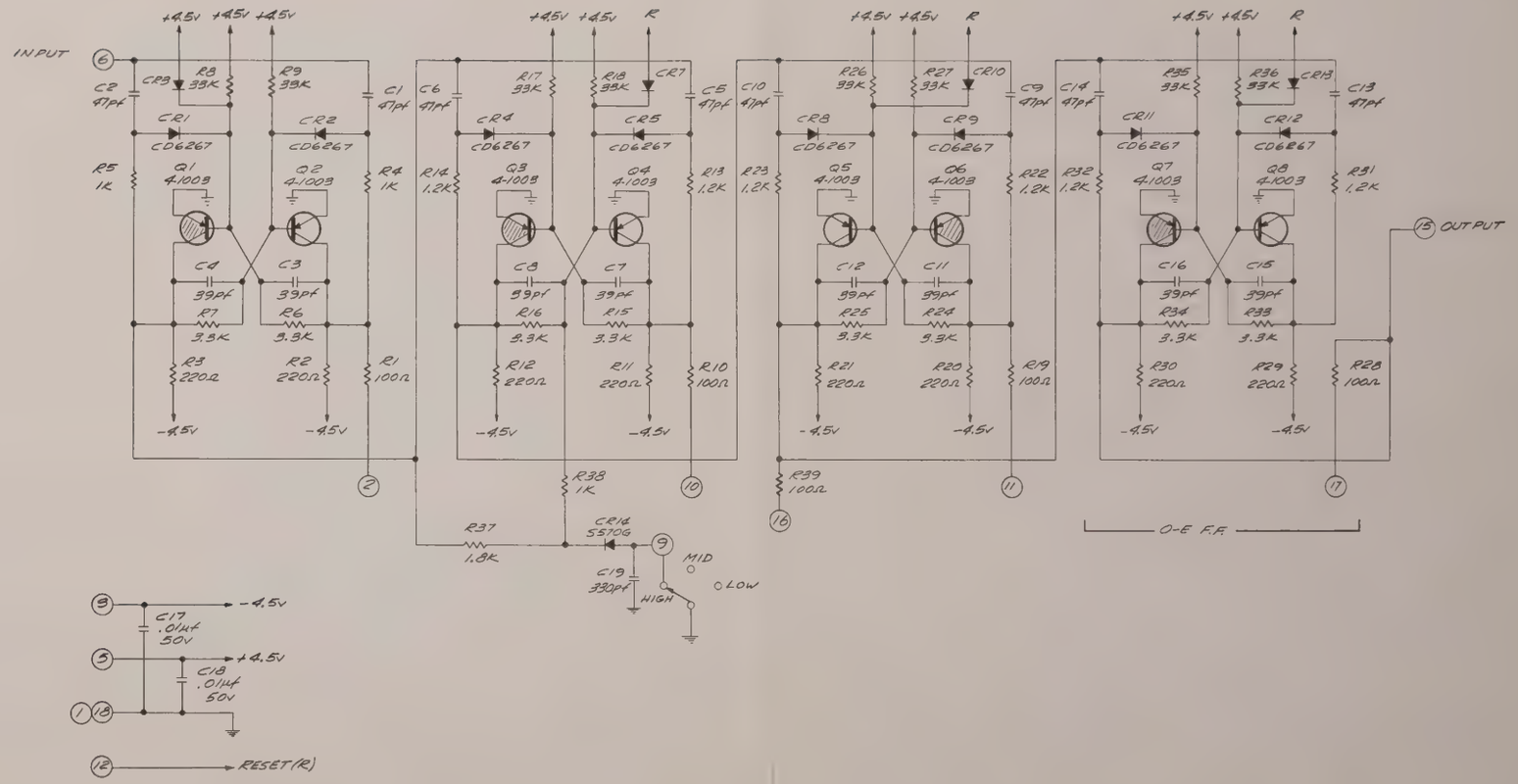




10-3448
SCHEMATIC, "A" LOGIC
J.A.I. 4-18-66

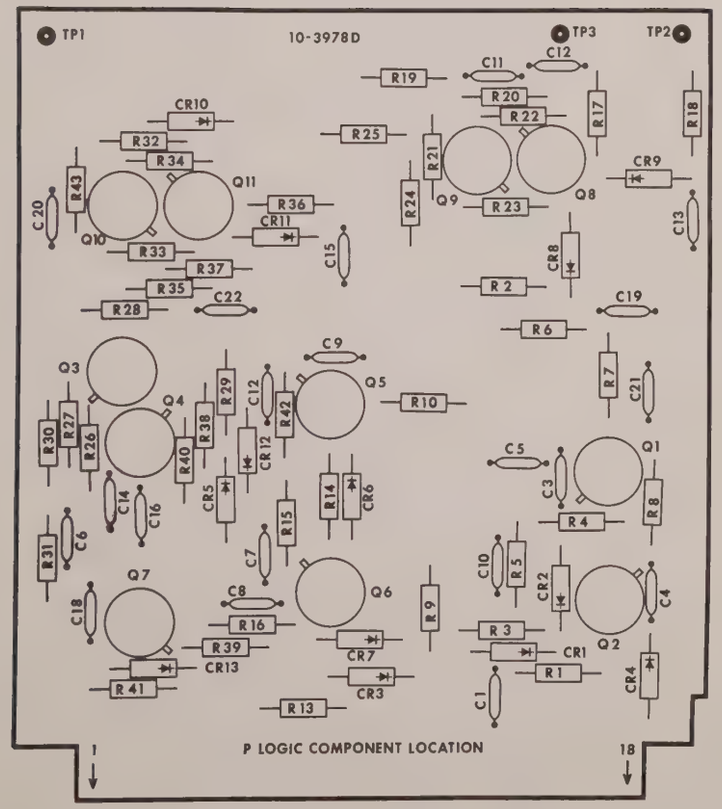
FIGURE 36 A LOGIC
SCHEMATIC DIAGRAM & COMPONENT LOCATION

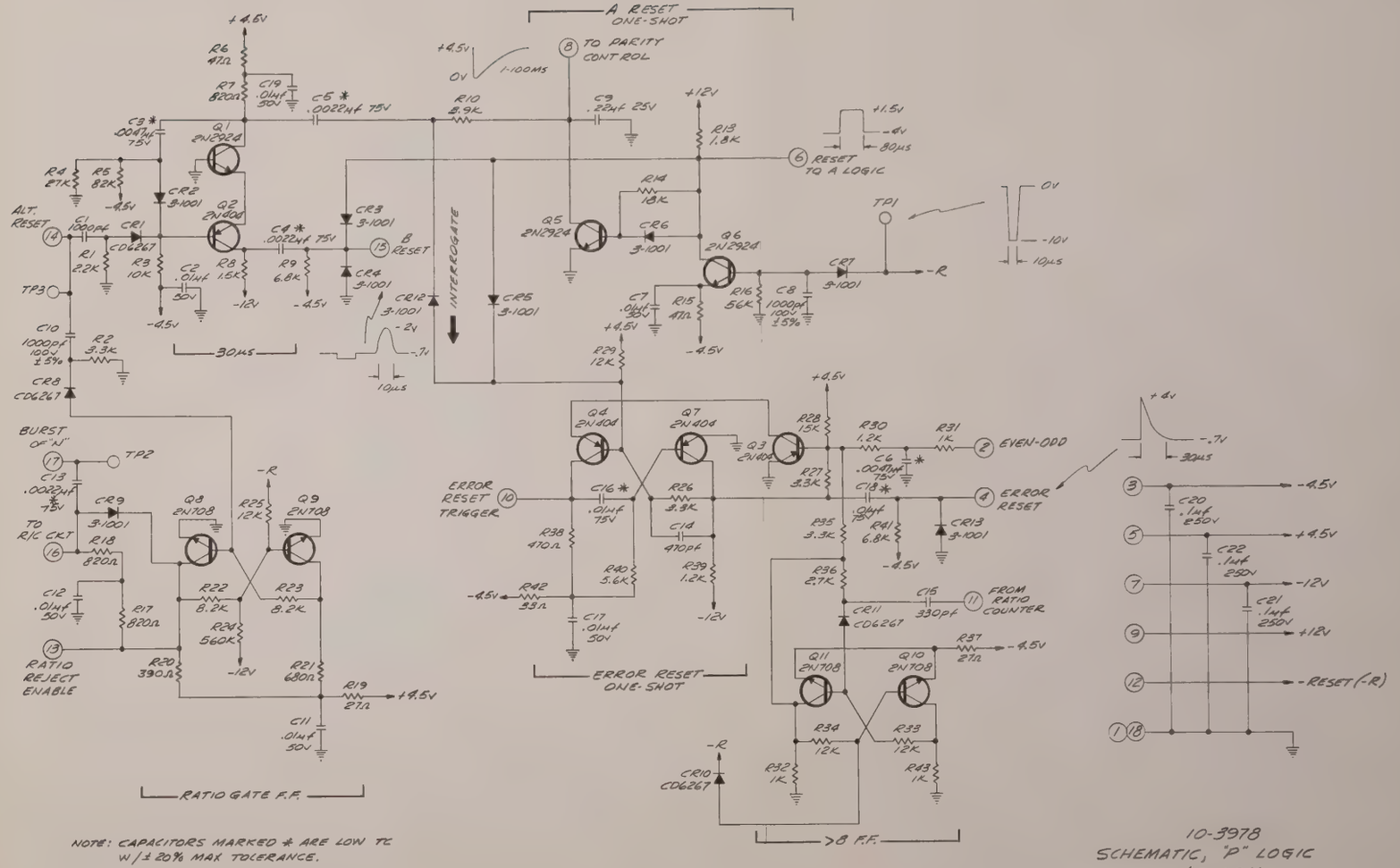




10-3449
SCHEMATIC, "B" LOGIC
J.A.I. 4-21-66

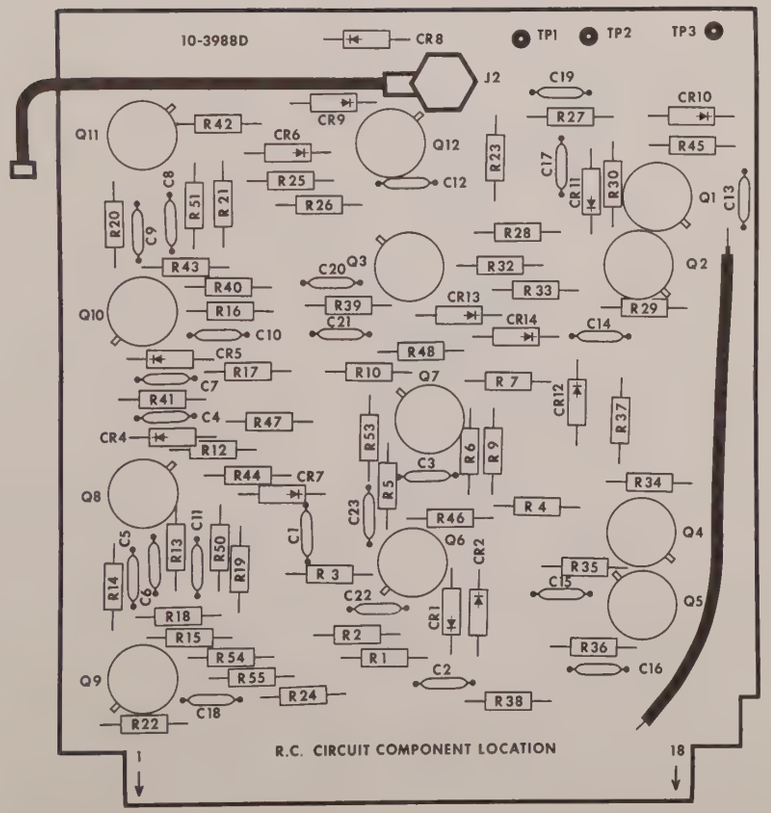
FIGURE 37 B LOGIC
SCHEMATIC DIAGRAM & COMPONENT LOCATION

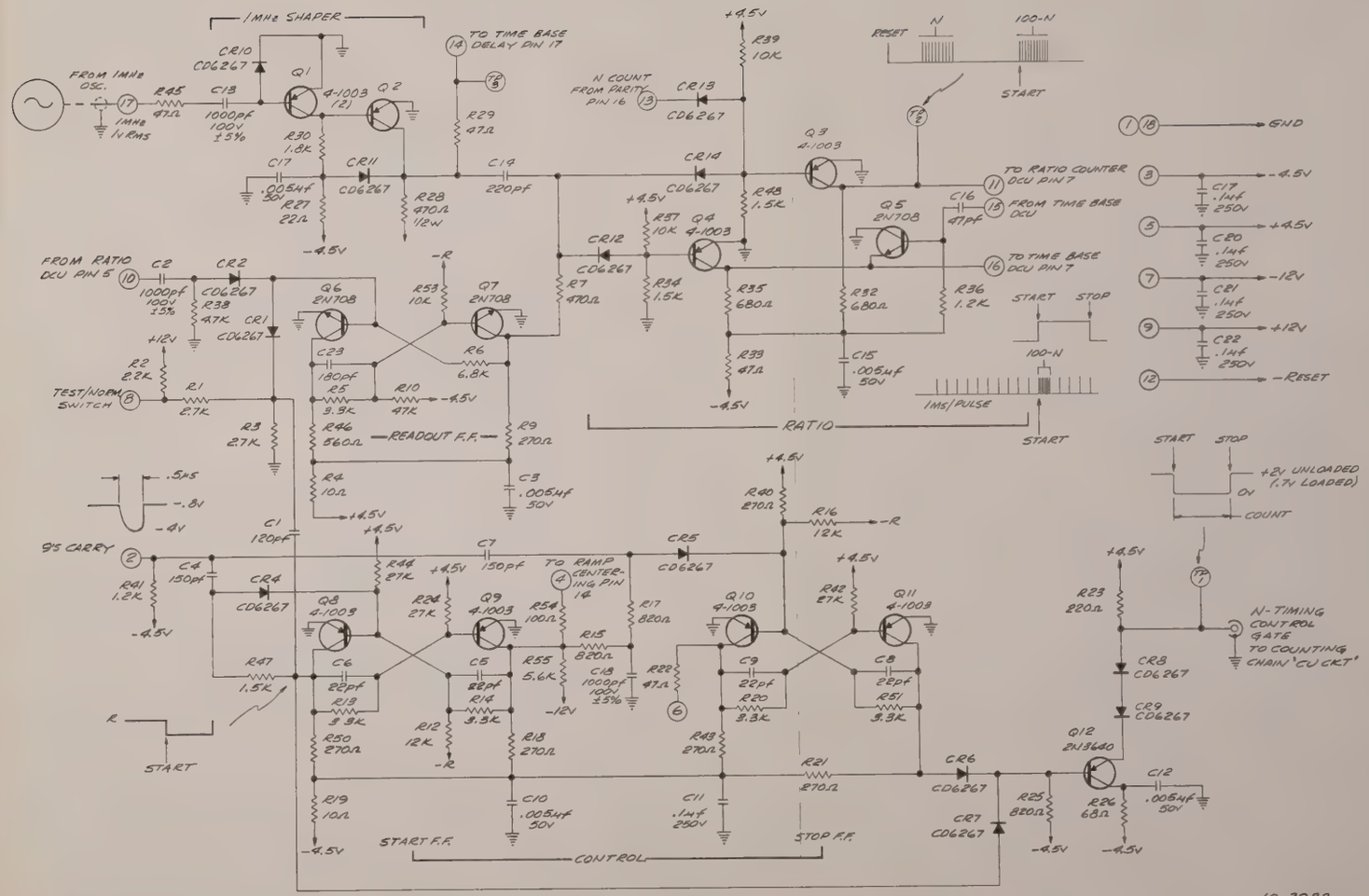




10-3978
SCHEMATIC, "P" LOGIC
JAI 5-2-66

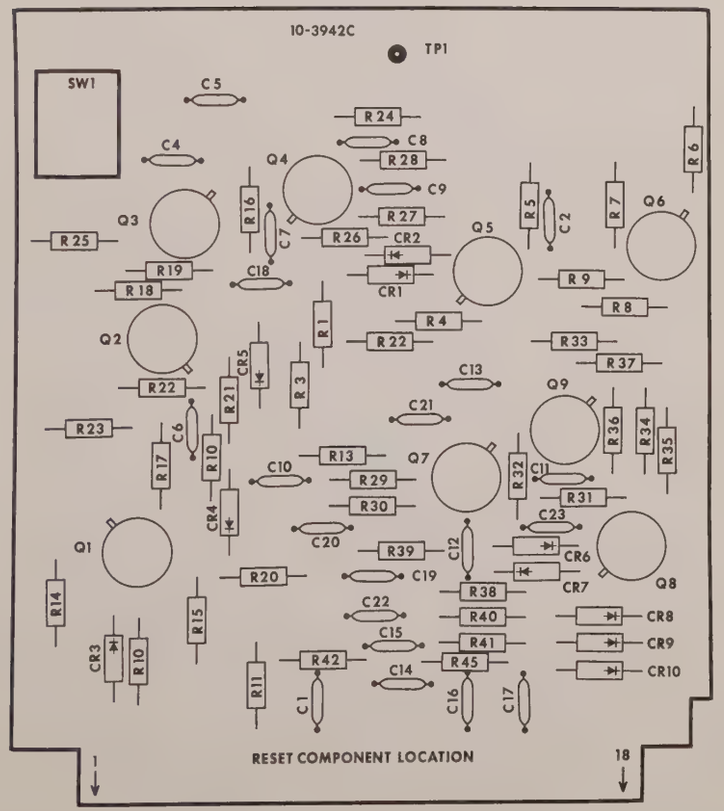
FIGURE 38 PARITY LOGIC
SCHEMATIC DIAGRAM & COMPONENT LOCATION

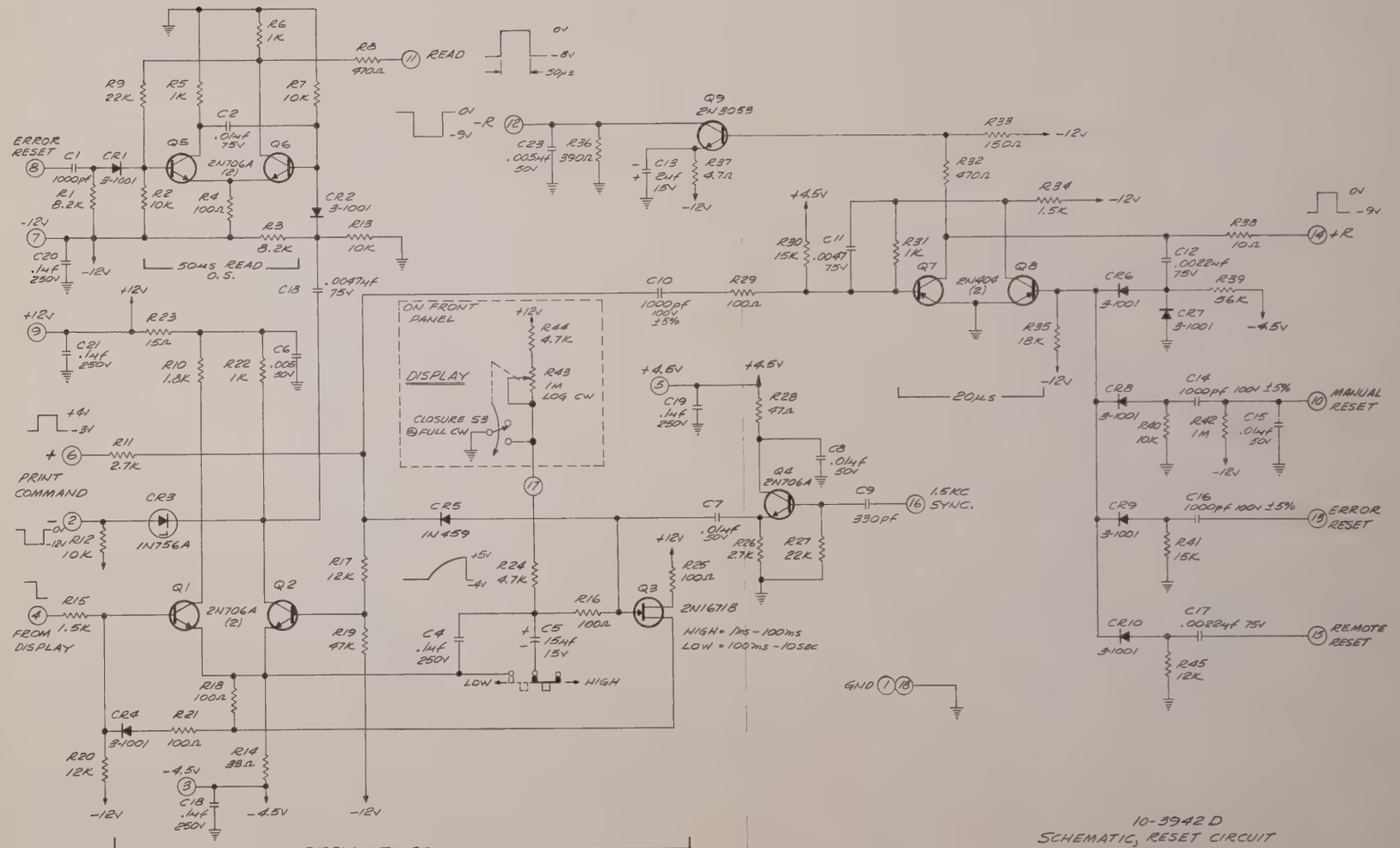




10-3988
SCHEMATIC, RATIO & CONTROL
J.A.I. 4-4-66

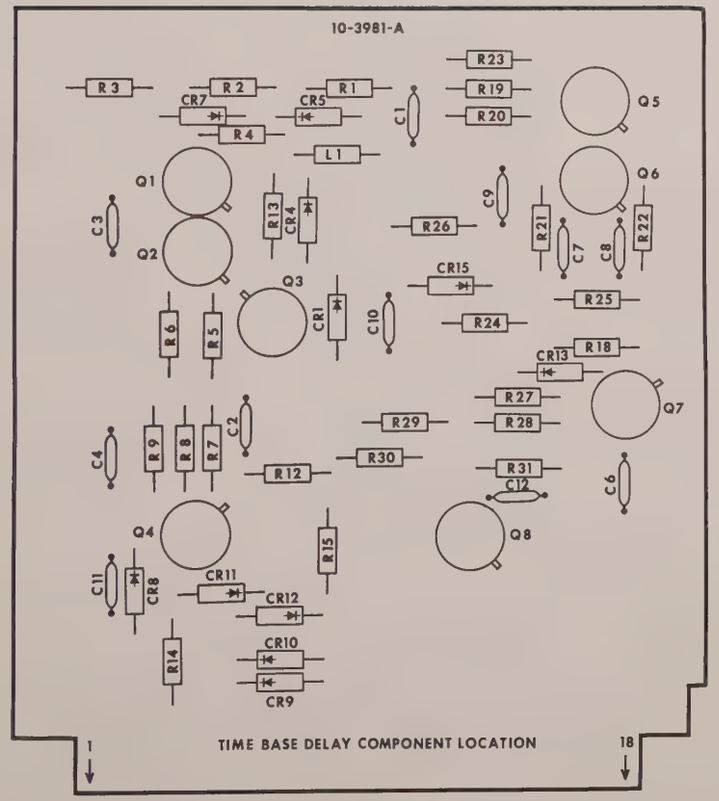
FIGURE 39 RATIO AND CONTROL CIRCUIT SCHEMATIC DIAGRAM & COMPONENT LOCATION

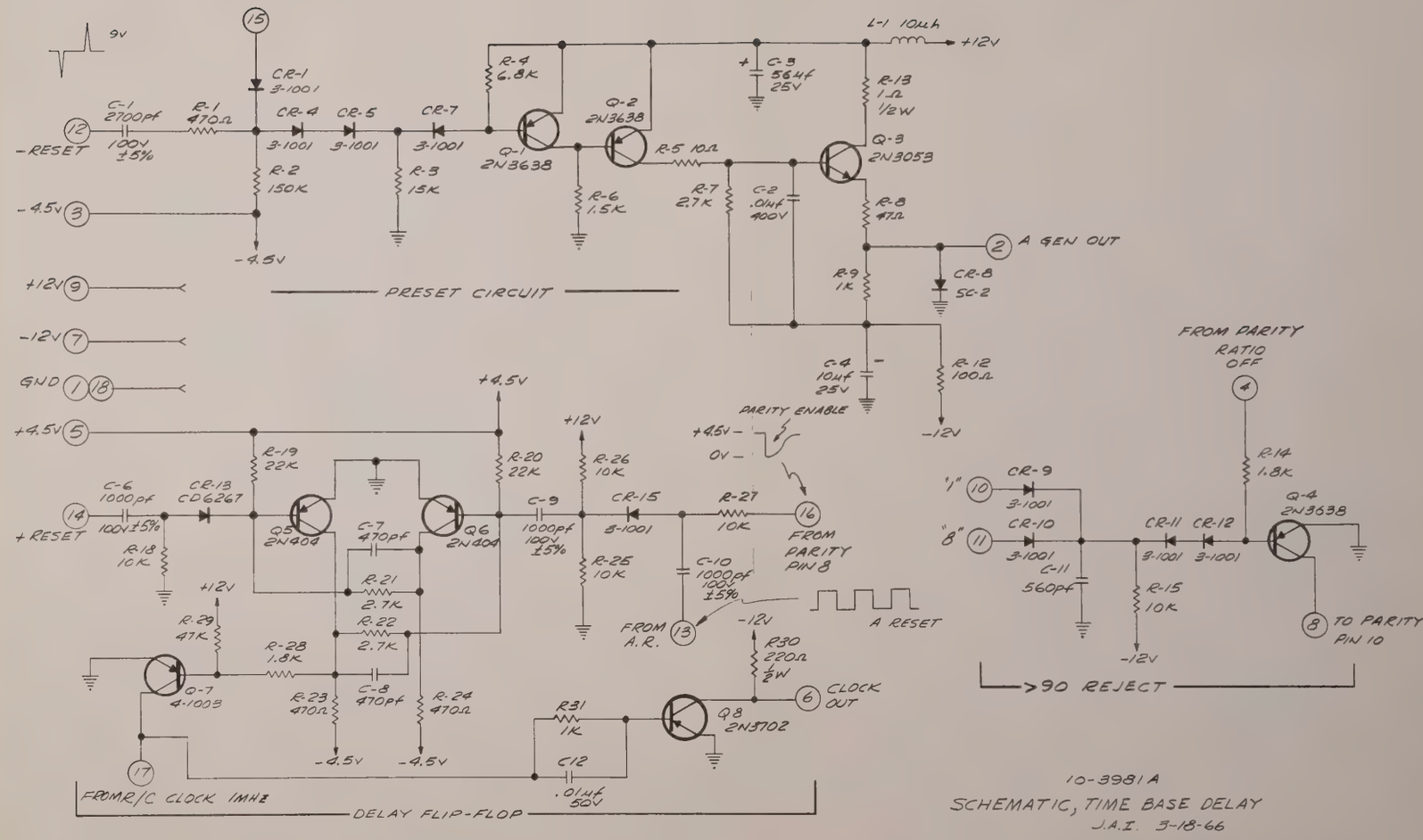




10-3942 D
SCHEMATIC, RESET CIRCUIT
J.A.I. 3-25-66

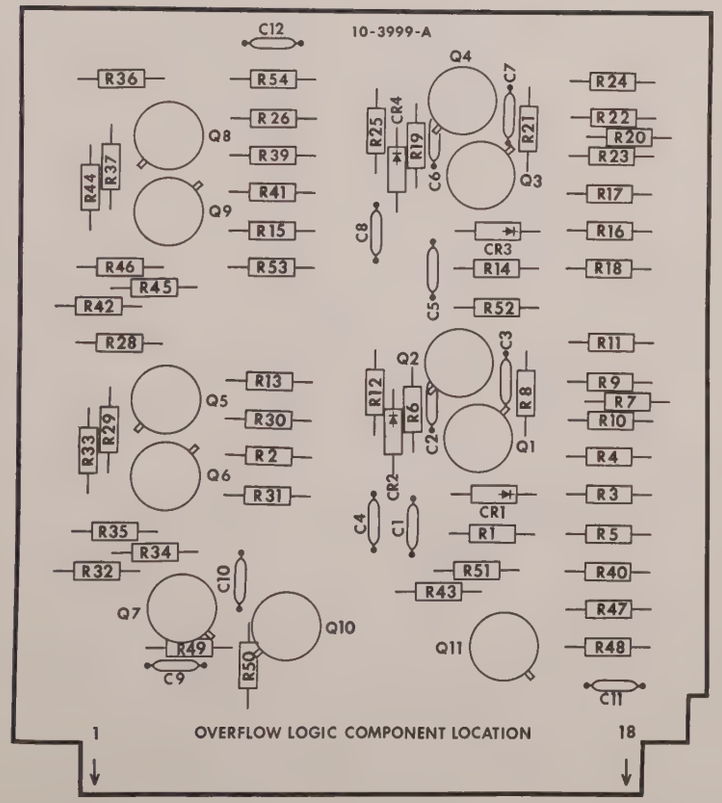
FIGURE 40 RESET CIRCUIT
SCHEMATIC DIAGRAM & COMPONENT LOCATION

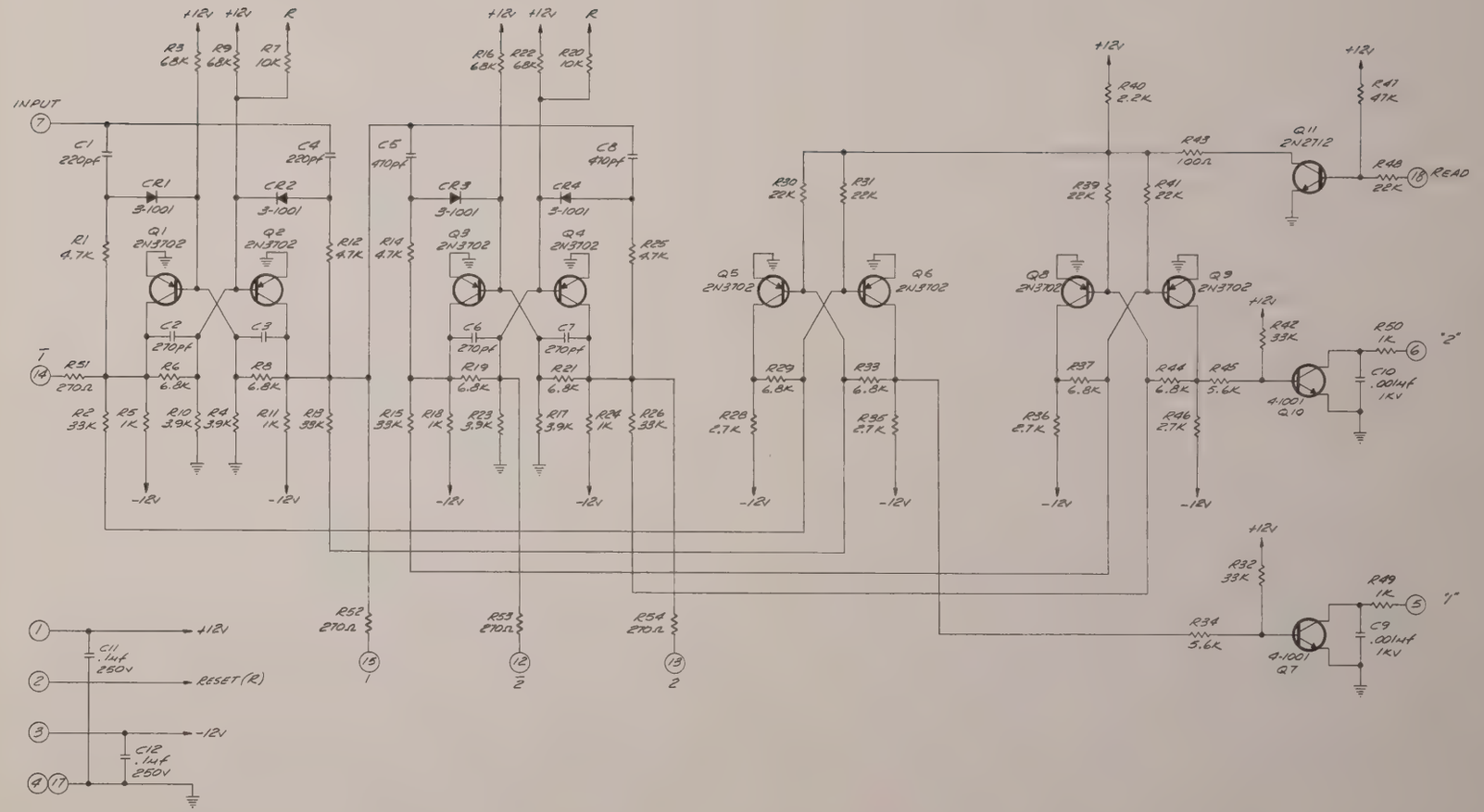




10-3981 A
SCHEMATIC, TIME BASE DELAY
J.A.I. 3-18-66

FIGURE 41 TIME BASE DELAY CIRCUIT
SCHEMATIC DIAGRAM & COMPONENT LOCATION





10-3999
SCHEMATIC, OVERFLOW LOGIC
JAI 5-3-66

FIGURE 42 OVERFLOW CIRCUIT
SCHEMATIC DIAGRAM & COMPONENT LOCATION

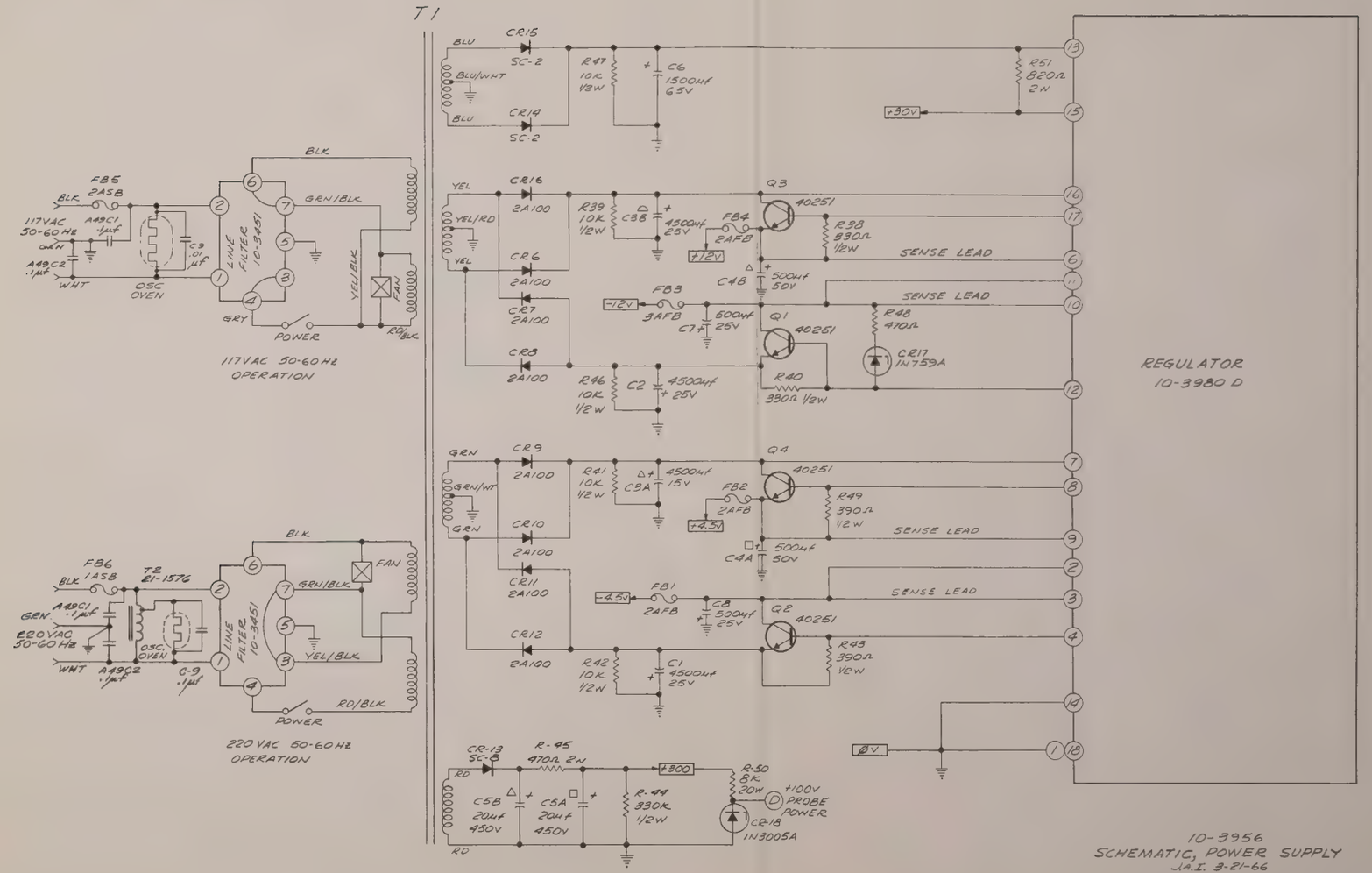
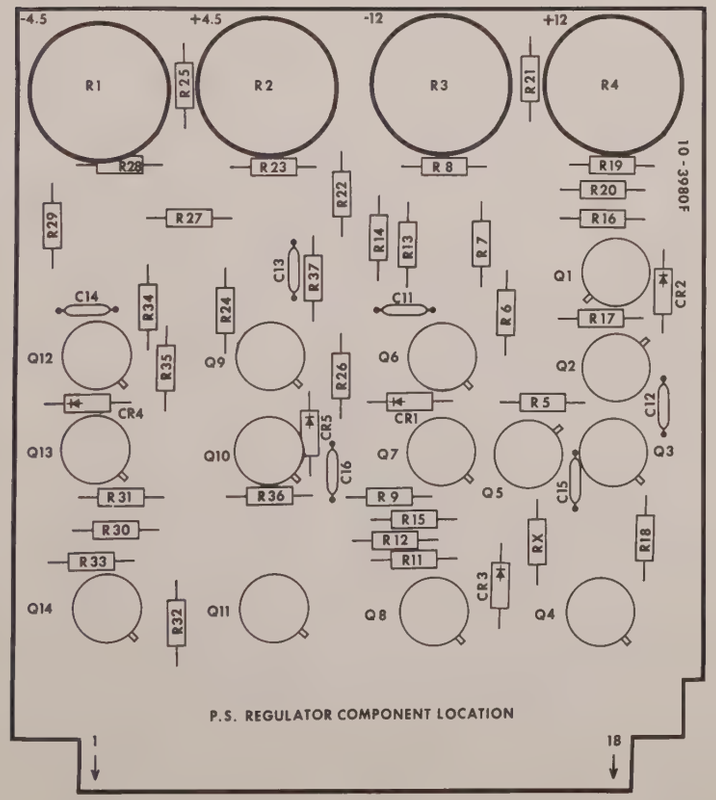


FIGURE 43 POWER SUPPLY SCHEMATIC DIAGRAM



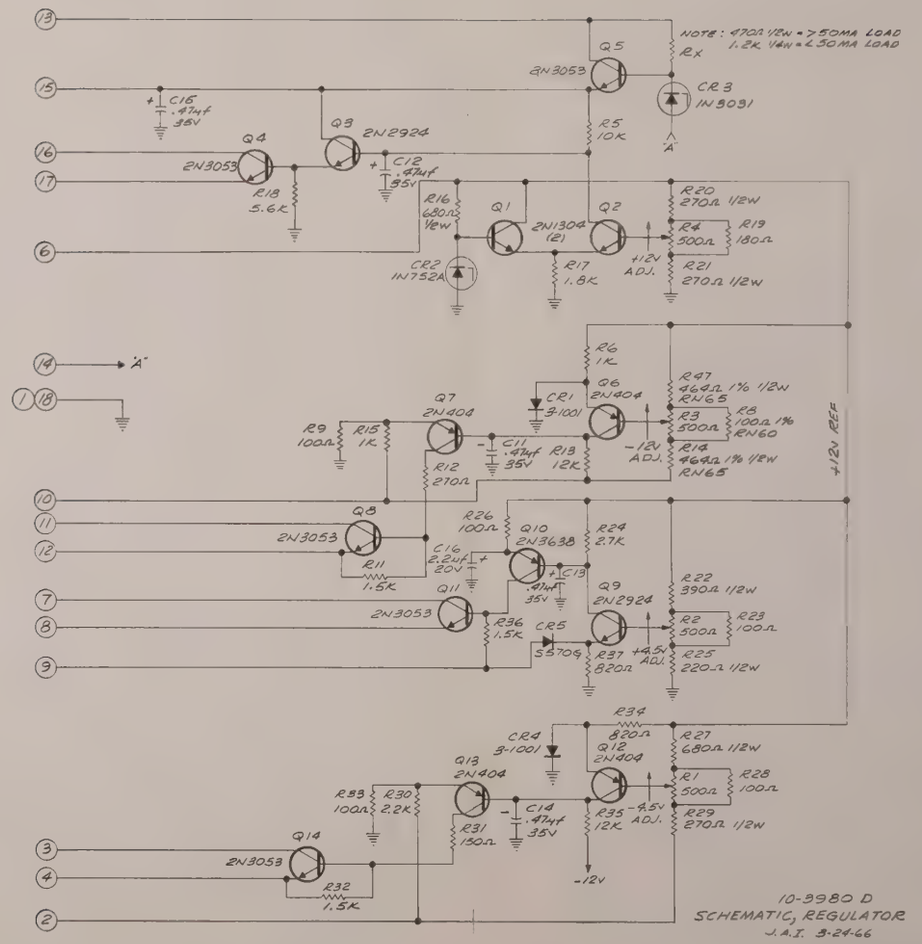


FIGURE 44 POWER SUPPLY REGULATOR
SCHEMATIC DIAGRAM & COMPONENT LOCATION

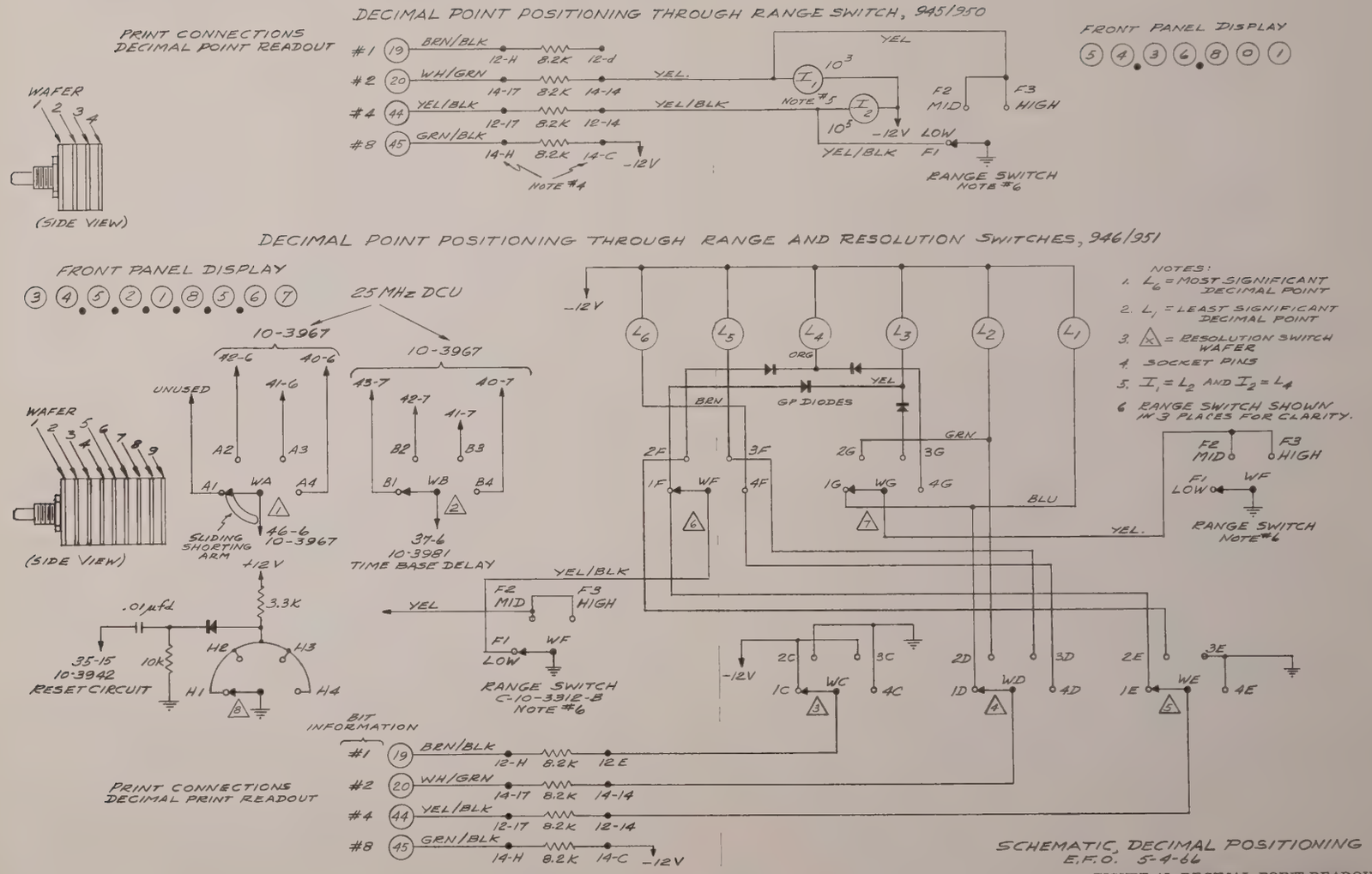


FIGURE 45 DECIMAL POINT READOUT SWITCH CONNECTIONS

PCB* CHASSIS LOCATION 945/950

1.	F.S. Circuit 10-3982	24.	F.S. Circuit 10-3982
2.	Blank	25.	A Logic 10-3414
3.	I.C. Circuit 10-3994	26.	P Logic 10-3978
4.	S.C. Circuit 10-3948	27.	B Logic 10-3415
5.	CU Circuit 10-3993	28.	CU Circuit 10-3993
6.	Memory Readout 10-4000	29.	Gate & Centering Circuit 10-3991
7.	Matrix Circuit 10-3933	30.	Blank
8.	Memory Readout 10-4000	31.	I.S. Circuit 10-3963
9.	25 MHz DCU 10-3968	32.	R Generator (Option A) 10-3977
10.	Memory Readout 10-4000	33.	Divide-by-16 Circuit (Option A) 10-3412
11.	2.5 MHz DCU 10-3967	34.	AD & Divide-by-Eight Circuit (Option A) 10-3992
12.	Memory Readout 10-4000	35.	Reset Circuit 10-3942
13.	250 KHz DCU 10-3966	36.	Ratio and Control Circuit 10-3988
14.	Memory Readout 10-4000	37.	Time Base Delay Circuit 10-3981
15.	250 KHz DCU 10-3966	38.	2.5 MHz DCU 10-3967
16.	Memory Readout 10-4000	39.	250 KHz DCU 10-3966
17.	250 KHz DCU 10-3966	40.	Blank
18.	Memory Readout 10-4000	41.	Blank
19.	250 KHz DCU 10-3966	42.	2.5 MHz DCU 10-3967
20.	Blank	43.	2.5 MHz DCU 10-3967
21.	Overflow Circuit (Option F) 10-3999	44.	2.5 MHz DCU 10-3967
22.	Blank	45.	2.5 MHz DCU 10-3967
23.	Blank	46.	2.5 MHz DCU 10-3967

*PCB = Printer Circuit Board

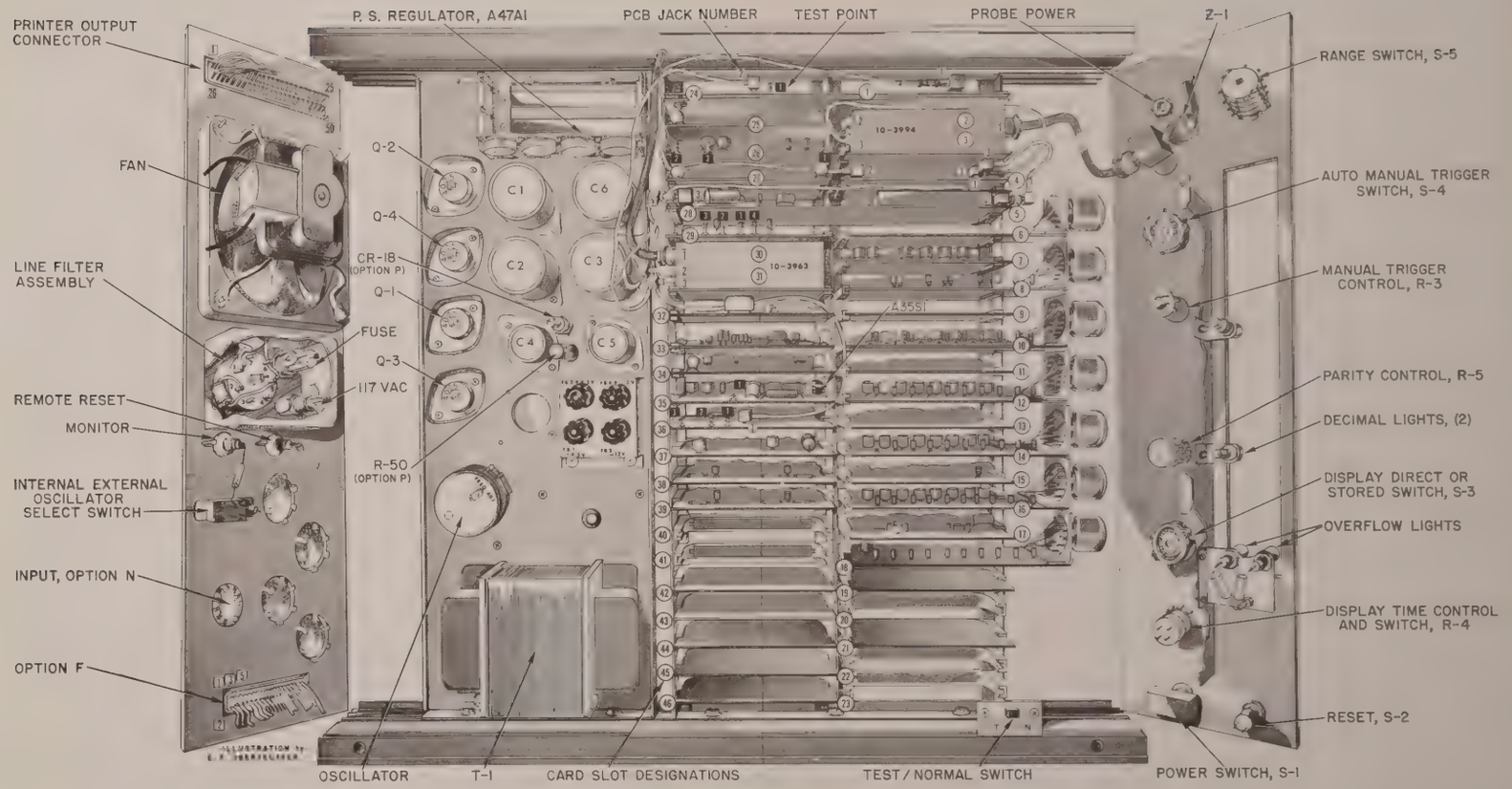


FIGURE 46. TOP ASSEMBLY AND COMPONENT LOCATION, 945/950

PCB* CHASSIS LOCATION 946/951

1.	F.S. Circuit 10-3982	24.	F.S. Circuit 10-3982
2.	Blank	25.	A Logic 10-3414
3.	I.C. Circuit 10-3994	26.	P Logic 10-3978
4.	S.C. Circuit 10-3948	27.	B Logic 10-3415
5.	CU Circuit 10-3993	28.	CU Circuit 10-3993
6.	Memory Readout 10-4000	29.	Gate & Centering Circuit 10-3991
7.	Matrix Circuit 10-3933	30.	Blank
8.	Memory Readout 10-4000	31.	I.S. Circuit 10-3963
9.	25 MHz DCU 10-3968	32.	R Generator (Option A) 10-3977
10.	Memory Readout 10-4000	33.	Divide-by-16 Circuit (Option A) 10-3412
11.	2.5 MHz DCU 10-3967	34.	AD & Divide-by-Eight Circuit (Option A) 10-3992
12.	Memory Readout 10-4000	35.	Reset Circuit 10-3942
13.	250 KHz DCU 10-3966	36.	Ratio and Control Circuit 10-3988
14.	Memory Readout 10-4000	37.	Time Base Delay Circuit 10-3981
15.	250 KHz DCU 10-3966	38.	2.5 MHz DCU 10-3967
16.	Memory Readout 10-4000	39.	250 KHz DCU 10-3966
17.	250 KHz DCU 10-3966	40.	2.5 MHz DCU 10-3967
18.	Memory Readout 10-4000	41.	2.5 MHz DCU 10-3967
19.	250 KHz DCU 10-3966	42.	2.5 MHz DCU 10-3967
20.	Memory Readout 10-4000	43.	2.5 MHz DCU 10-3967
21.	250 KHz DCU 10-3966	44.	2.5 MHz DCU 10-3967
22.	Memory Readout 10-4000	45.	2.5 MHz DCU 10-3967
23.	250 KHz DCU 10-3966	46.	2.5 MHz DCU 10-3967

*PCB = Printed Circuit Board

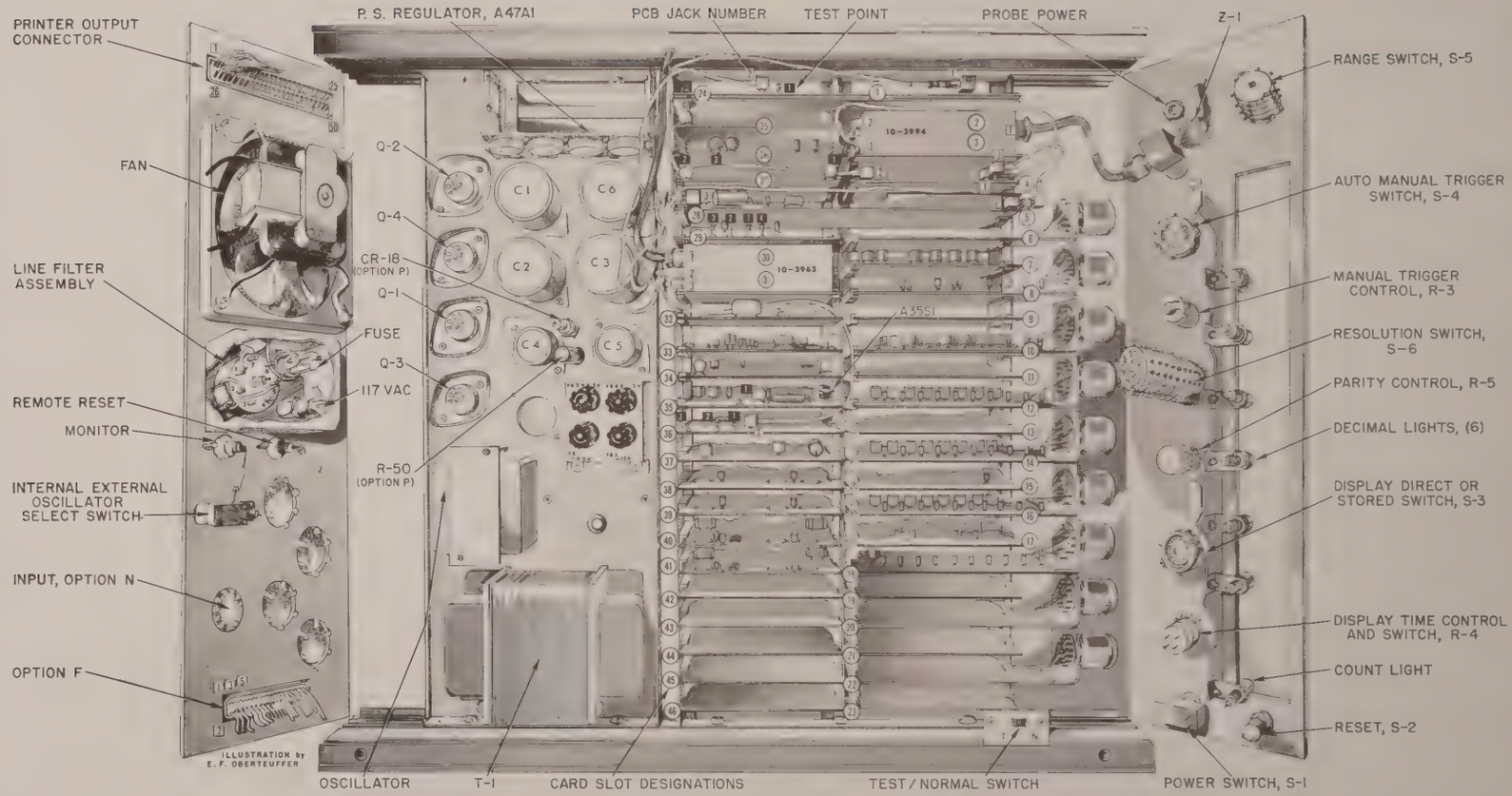


FIGURE 47. TOP ASSEMBLY AND COMPONENT LOCATION, 946/951

CALL OUT IDENTIFICATION

(1) = .1 uf	(9) = 6.8K
(2) = 50 uf 12 wvdc	(10) = 10K
(3) = 50 uf 25 wvdc	(11) = 1.8K
(4) = 33 uf	(12) = 390 Ohm
(5) = 2.2 uf	(13) = 1.2K
(6) = 3-1001 Diodes	(14) = 330 Ohm
(7) = CD6267 Diodes	(15) = 15K
(8) = 47K	(16) = 8.2K

(9)(4)= 9 is component value
(4) is number of components

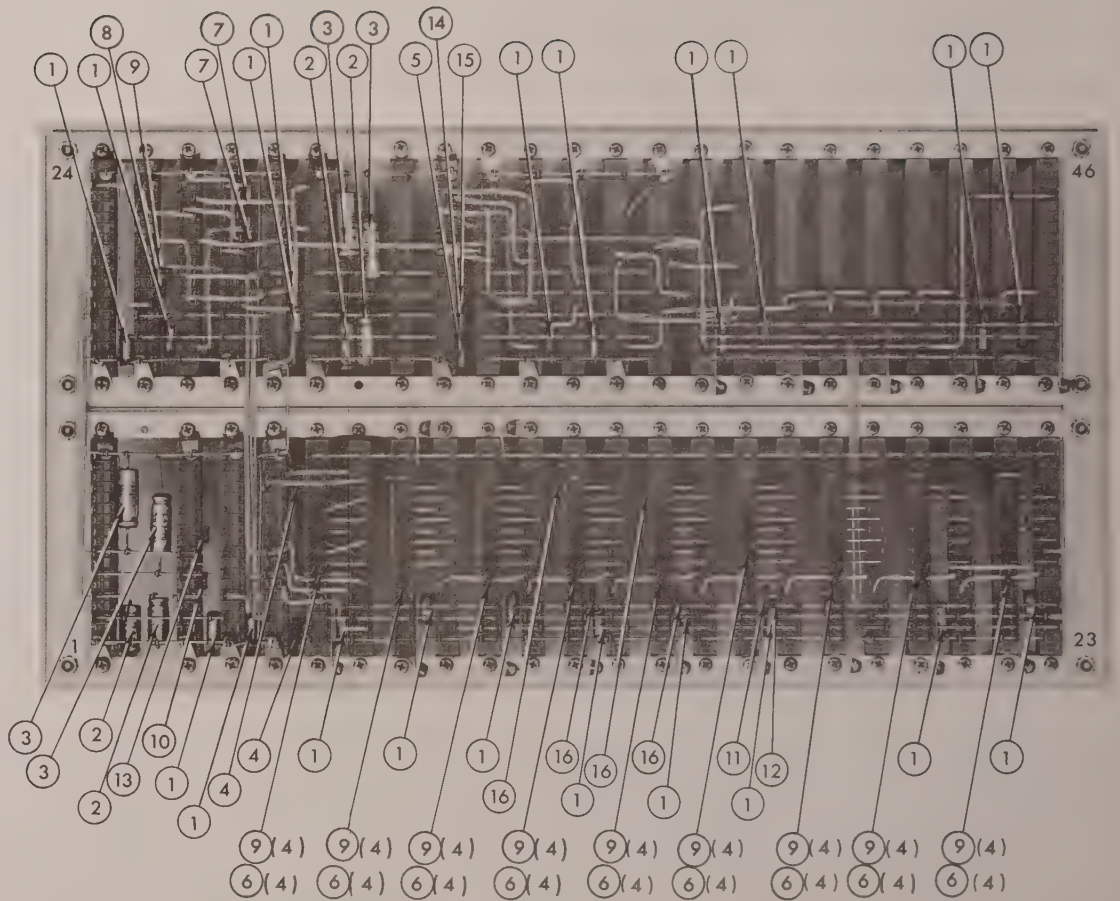
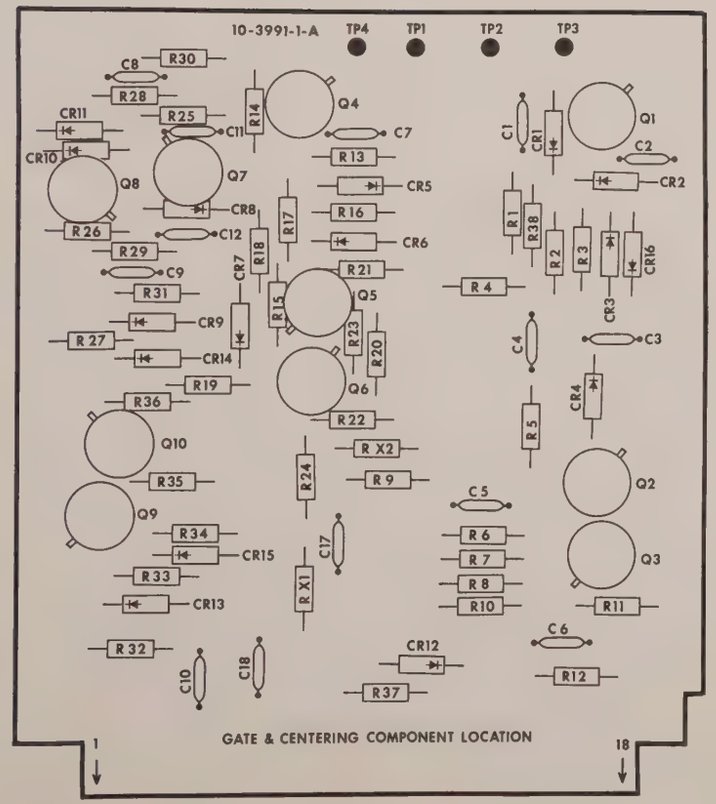


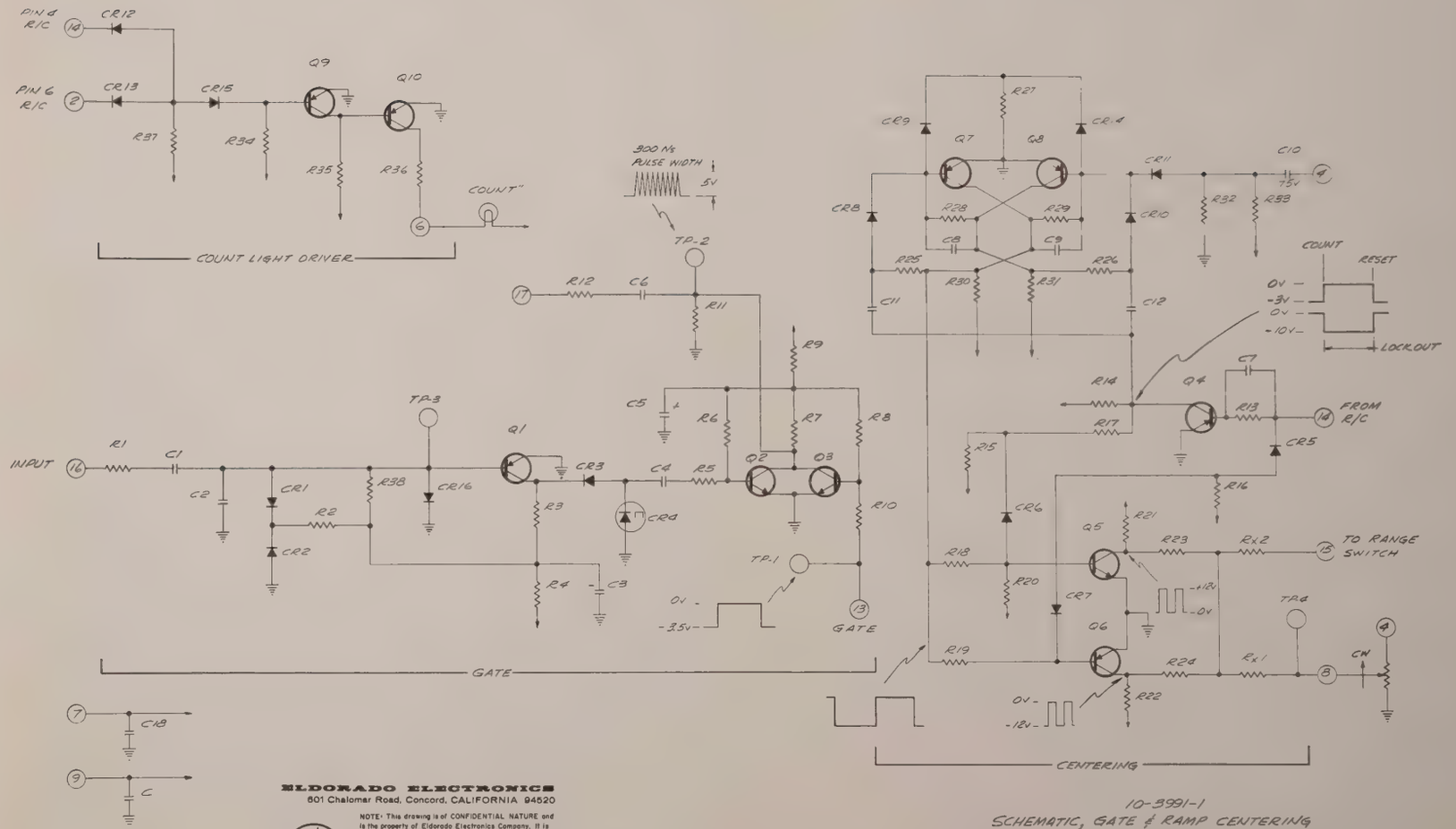
FIGURE 48 LOGIC CHASSIS
BOTTOM VIEW COMPONENT LOCATION

ADDENDUM

The following confidential drawings are added to this manual as a maintenance aid. In some drawings a portion of the assembly has been deleted and in all drawings component values have been deleted.

Direct replacement of the P.C. Board assembly is the recommended repair procedure. Replacement parts are available from Eldorado Electronics by identifying the component by part number and drawing circuit board name and number.





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10-3991-1
SCHEMATIC, GATE & RAMP CENTERING
J.A.I. 4-11-66

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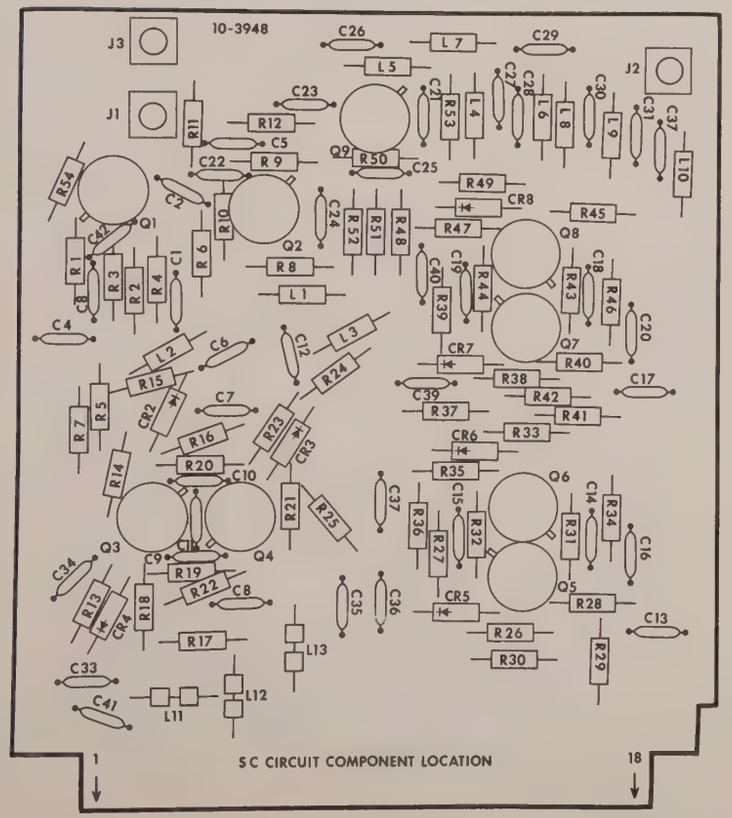

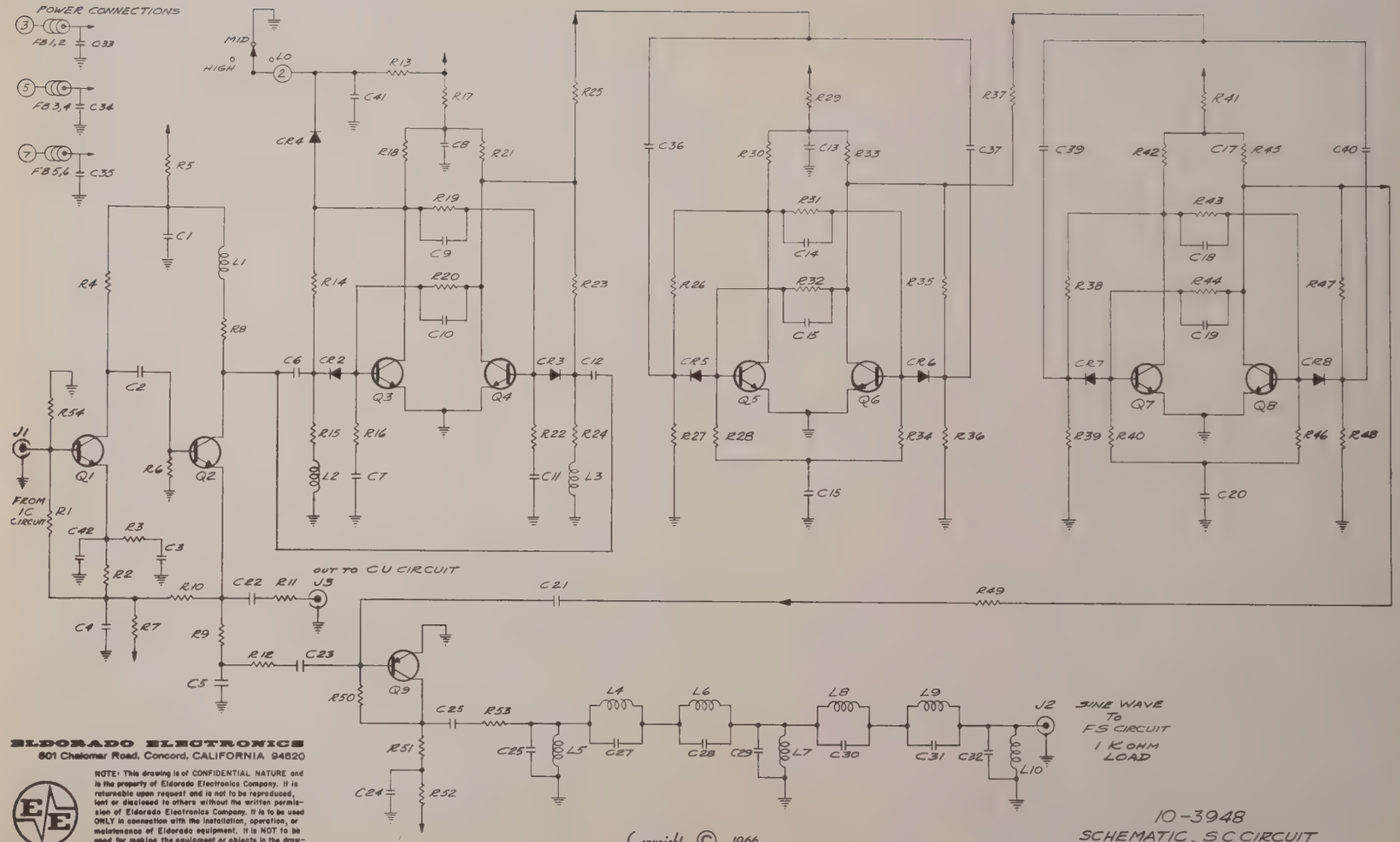

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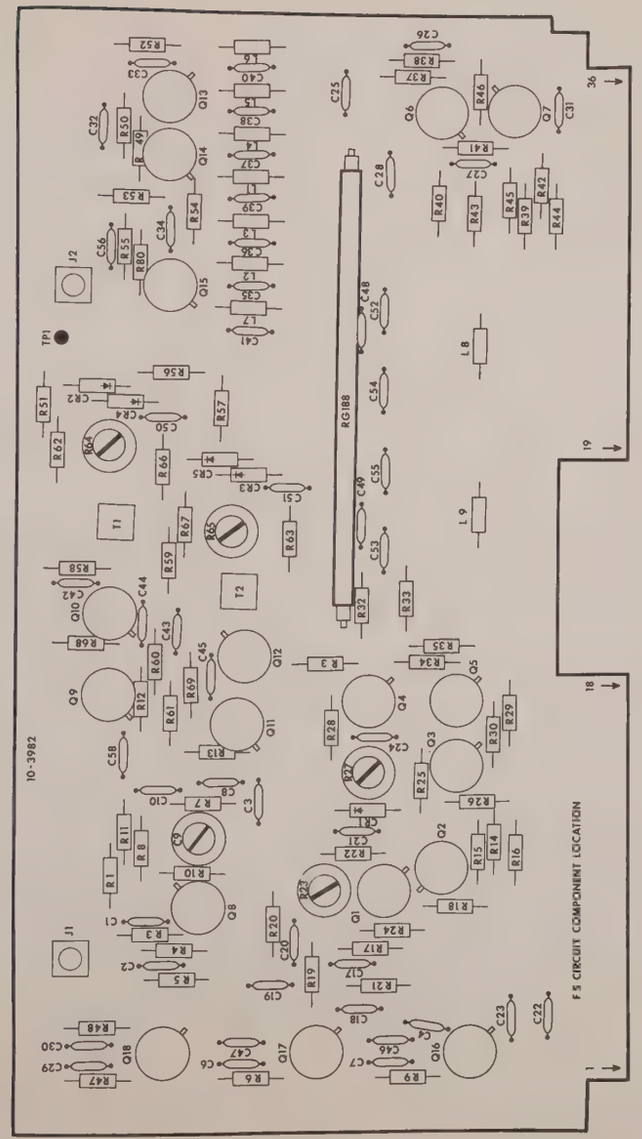
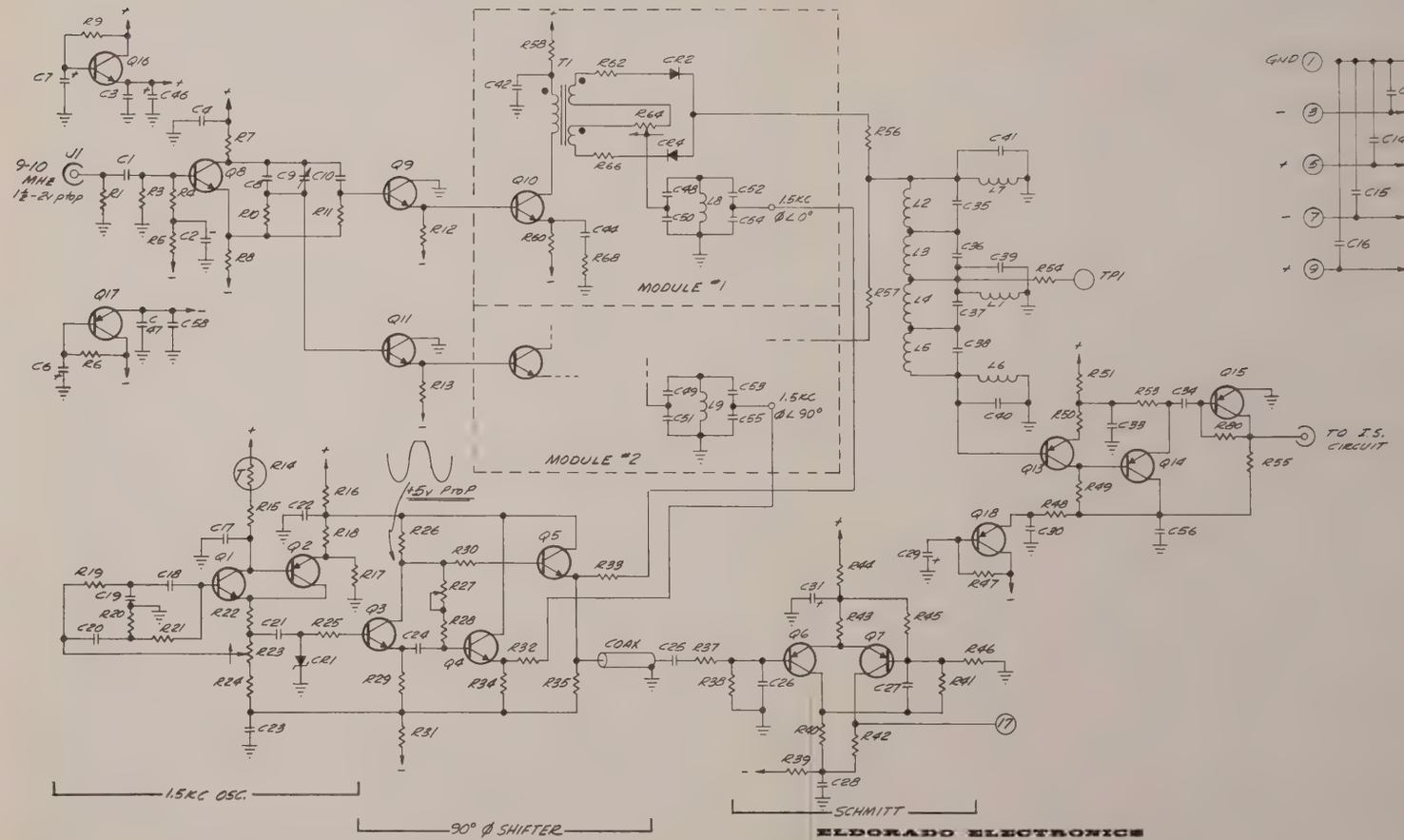
10-3948
SCHEMATIC, SC CIRCUIT
EFO 6-29-66





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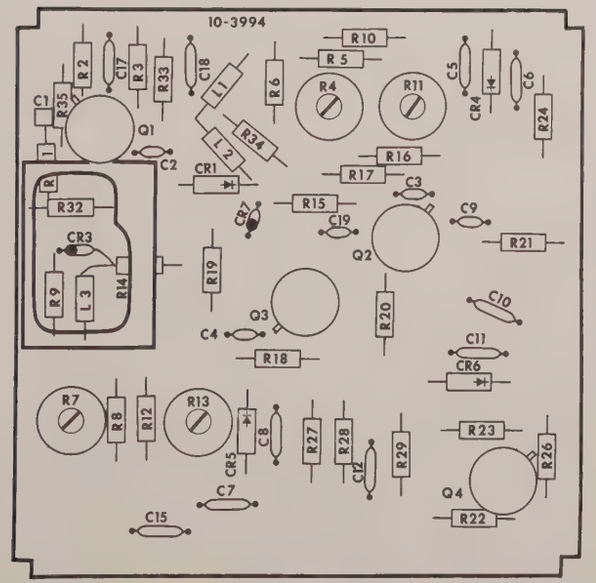
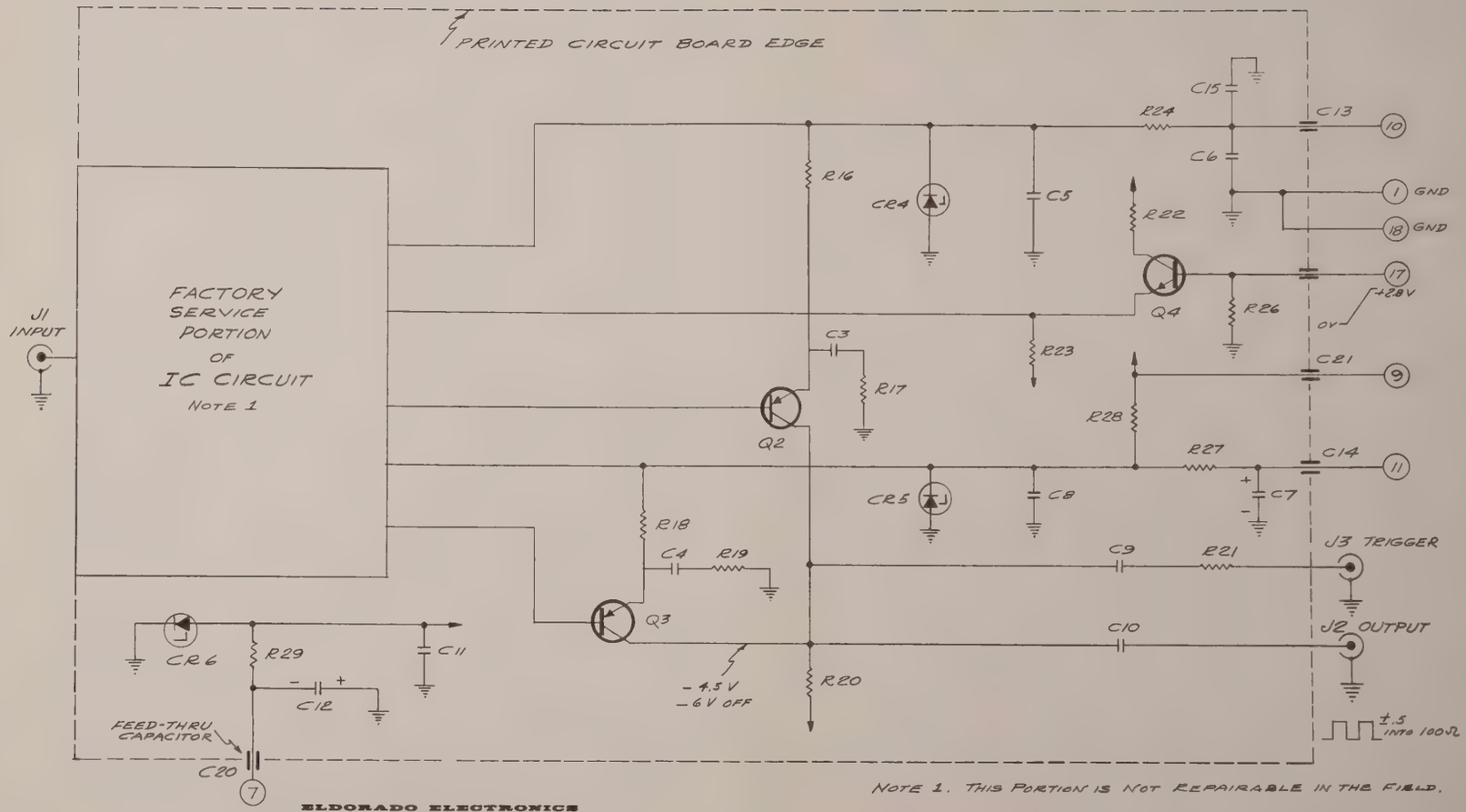
10-3982A
SCHEMATIC, F.S. CIRCUIT
J.A.I. 6-30-66



IC CIRCUIT COMPONENT LOCATION



NOTE 1. THIS PORTION IS NOT REPAIRABLE IN THE FIELD.

10-3994
SCHEMATIC, IC CIRCUIT
EFO 7-1-66

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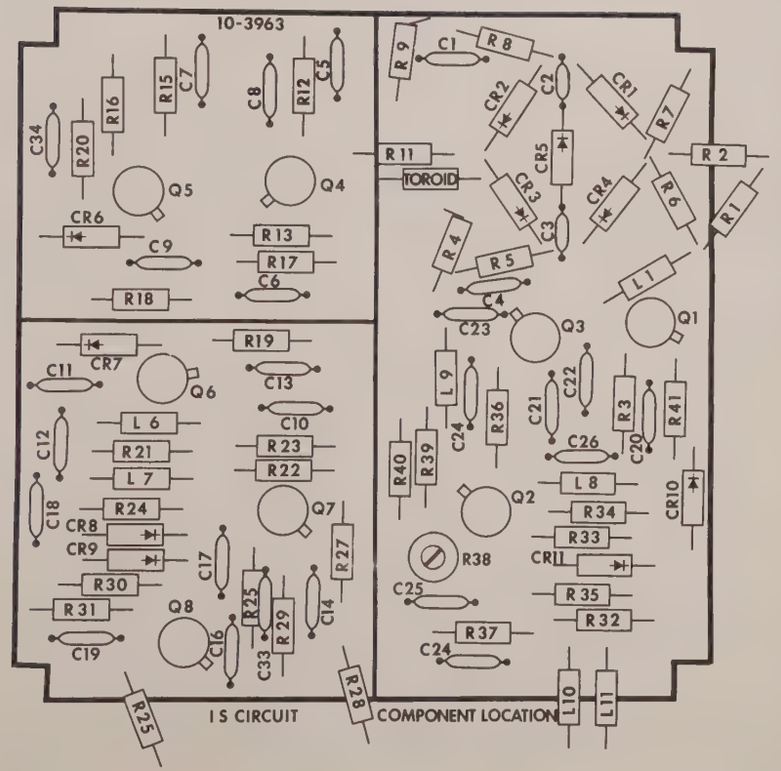

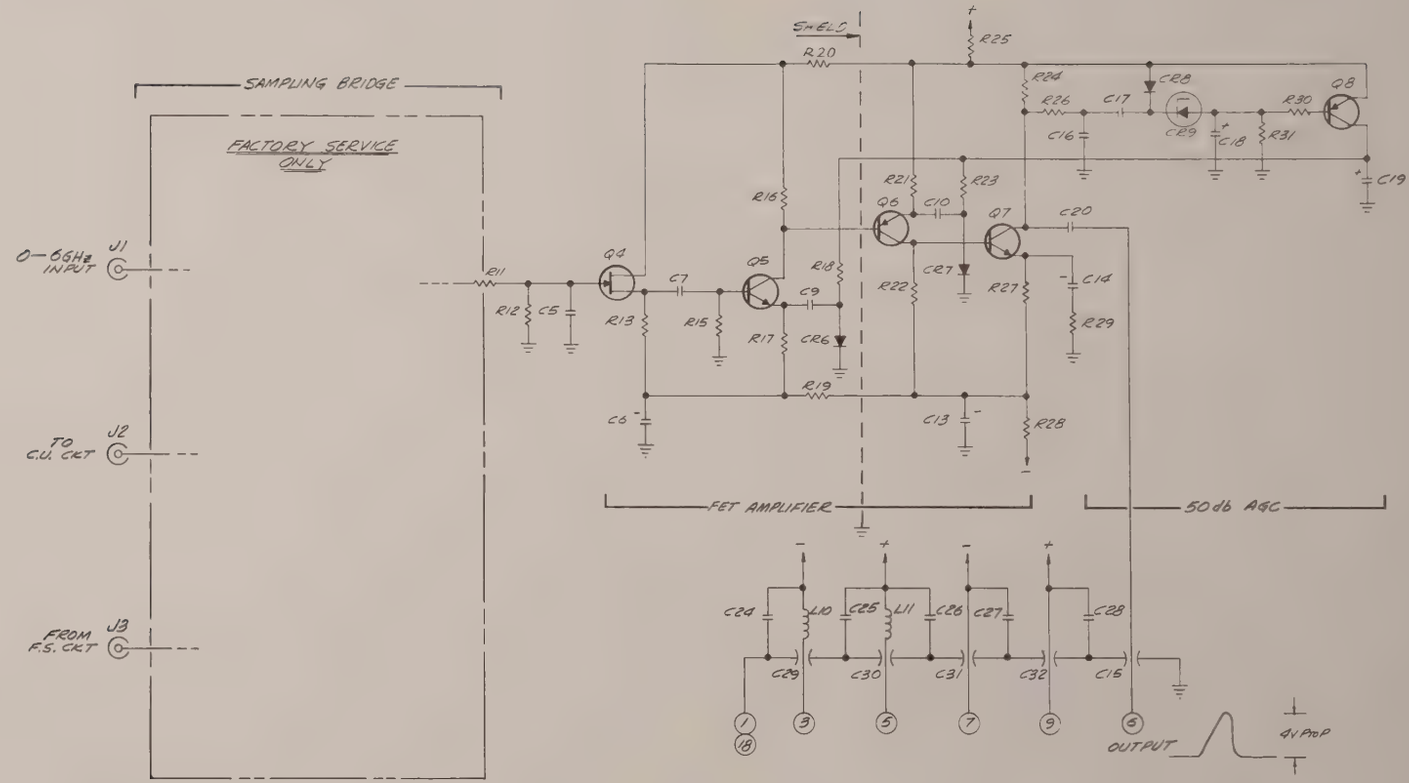

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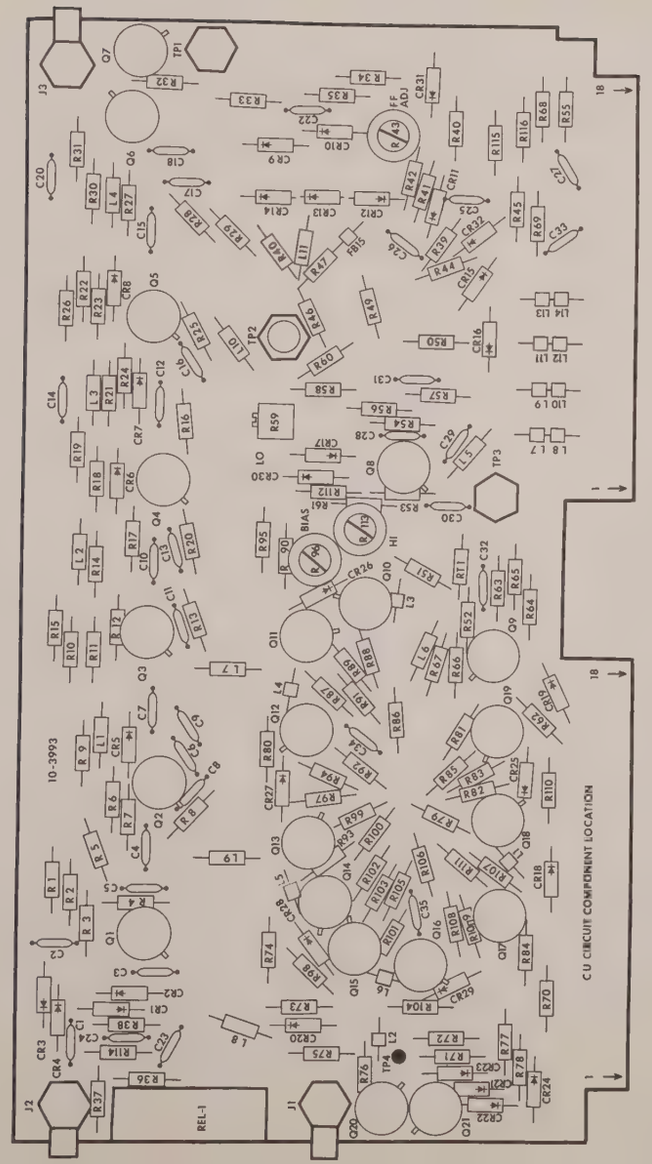
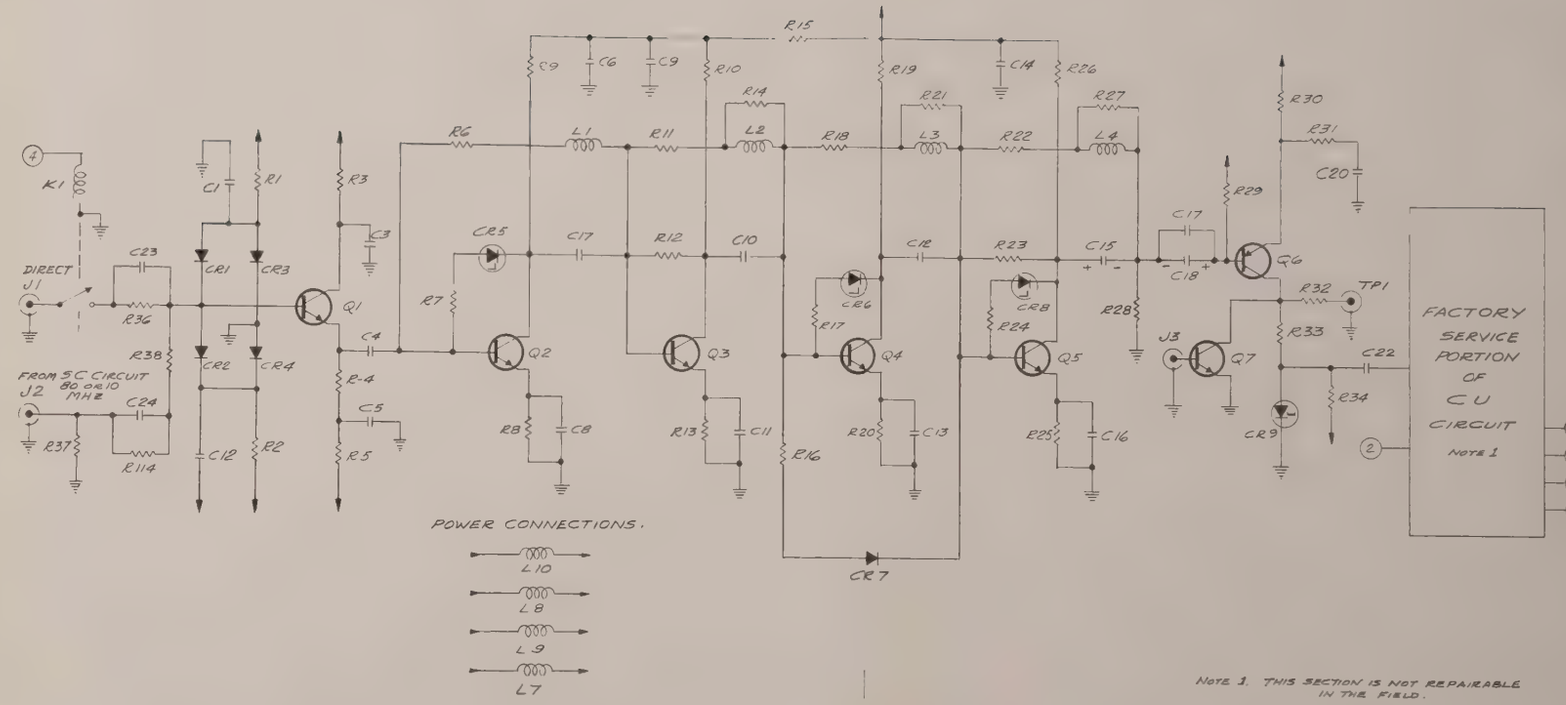
10-3973C
SCHEMATIC, I.S. CIRCUIT
JAI 7-8-66





NOTE 1. THIS SECTION IS NOT REPAIRABLE IN THE FIELD.

10-3993
SCHEMATIC, C U CIRCUIT
EFO 7-1-66

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